Integration tests with **G**lobal **M**uon **T**rigger

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CMS Trigger meeting
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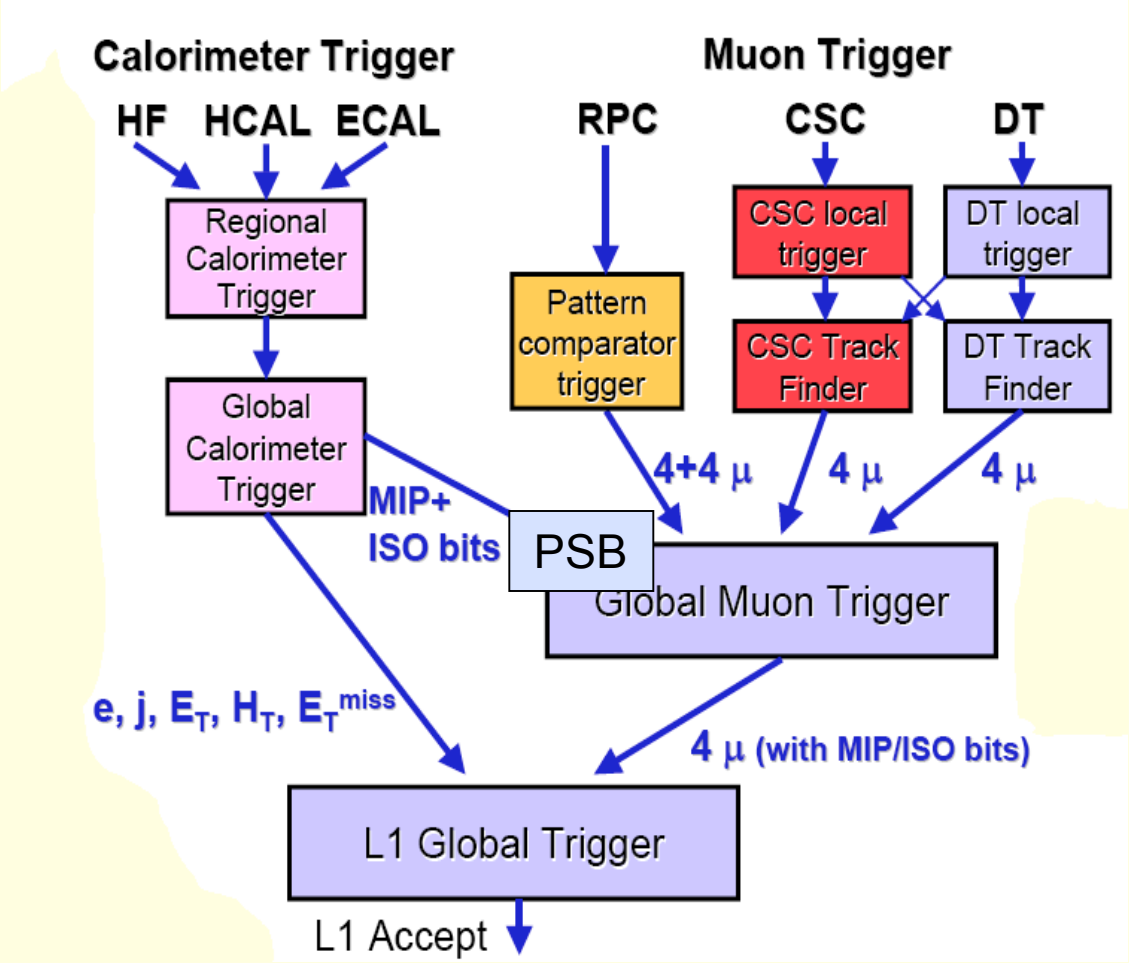
Overview

- GMT Integration tests
  - Tests with DTTF
  - Triangular DTTF-CSCTF-GMT test
  - Tests with PSB
- SW activities
- Conclusions



Tests with DTTF

- End of January: tests with bit patterns sent from **Wedge Sorter** (WS) through **Barrel Sorter** (BS) into **GMT** were successful
- Using common clock from **TTCci** and **TTCex**
- In February the **PHTF** board was added to the chain
- Muon track segments generated with ORCA (by Jorge) were injected into the PHTF using the **DIO** (auxiliary pattern injector)
- At the inputs of the GMT data were compared to the expected values
- Long term tests (hours) were performed in real time coparing data in Input FPGA's every orbit against the data stored from the first orbit.

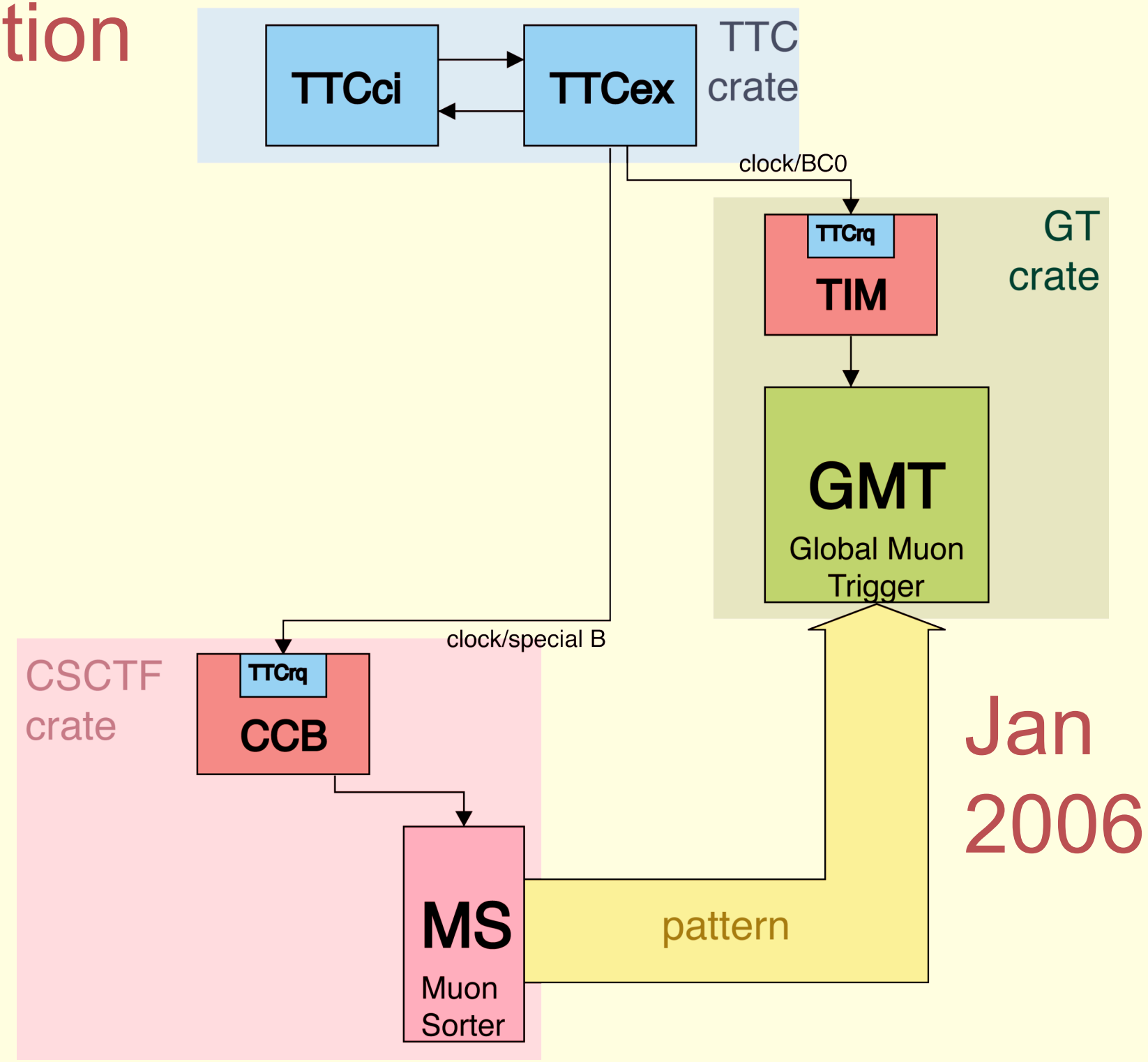
Results of tests with DTTF

- **WS-BS-GMT**:
  - Pattern tests were successful.
- **DIO-PHTF-WS-BS-GMT**:
  - Correct timing becomes very important: accumulated jitter decreases the size of the valid clock-phase window
  - After a thorough timing setup, long term tests with ORCA data showed a few bit errors/hour. The main reason was traced down to DIO instability and DIO-PHTF connection (DIO is not part of the final system however). Improvements are foreseen (Janos).

DTTF-CSCTF-GMT tests

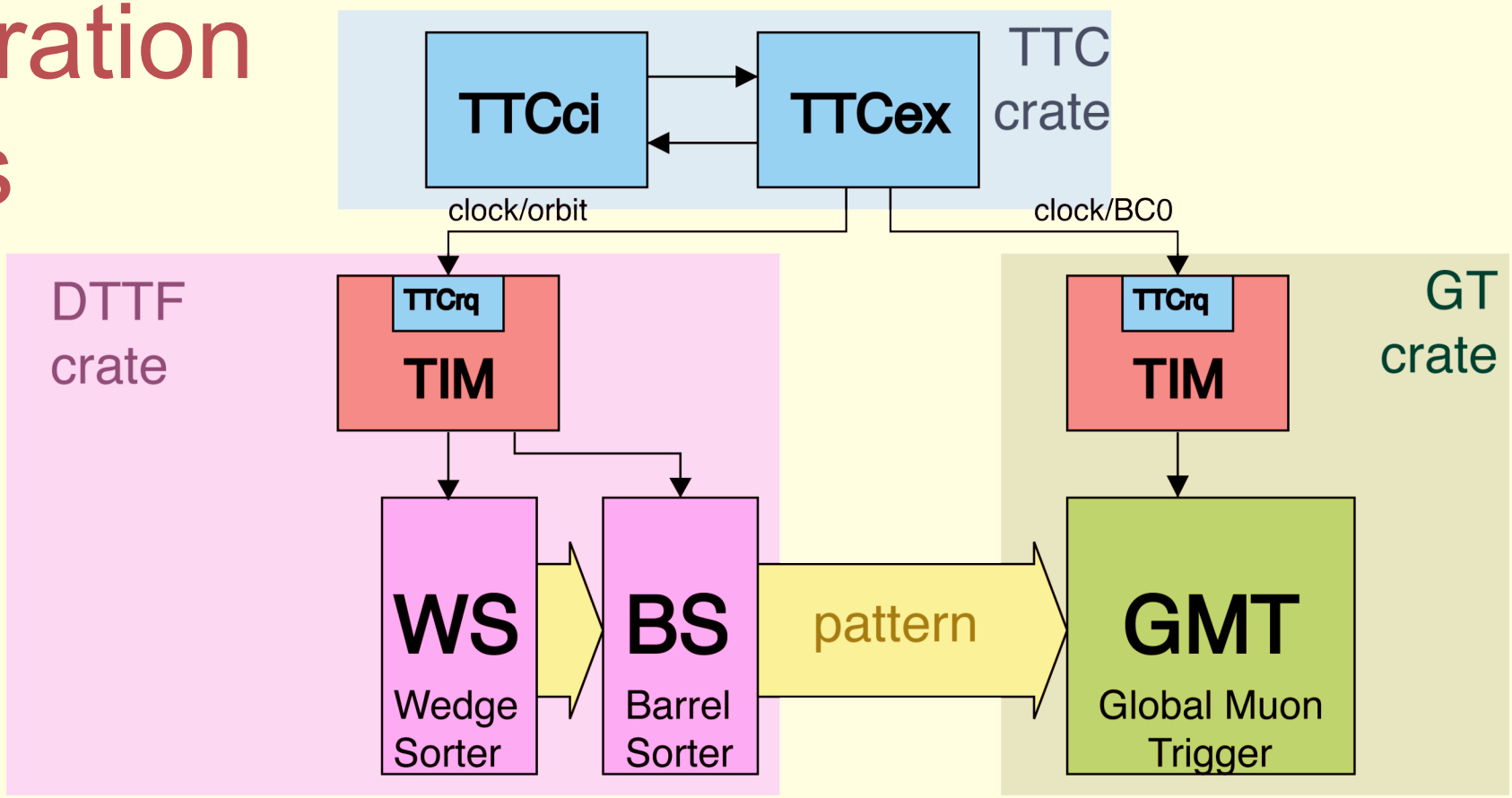
- This triangular test is under preparation:
  - Timing has been tested using a common TTCci/TTCex source by injecting muon track fragments at given bunch crossing to both DTTF(only PHTF) and CSCTF. Track segments are exchanged between DTTF and CSCTF. After track-building both TF's send the resulting track via their respective Sorters to GMT. At GMT inputs the data are resynchronised and read.
  - Specially filtered ORCA data is under preparation (Jorge, Janos, Dan, I.). It has to reflect the availability of individual modules (only one phi sector, no ETTF, etc.)
- It is planned to perform this test during upcoming weeks. Using modified LUT's in GMT one could test also the cancel-out functionality (was tested up to now only in a selftest)

Integration Tests



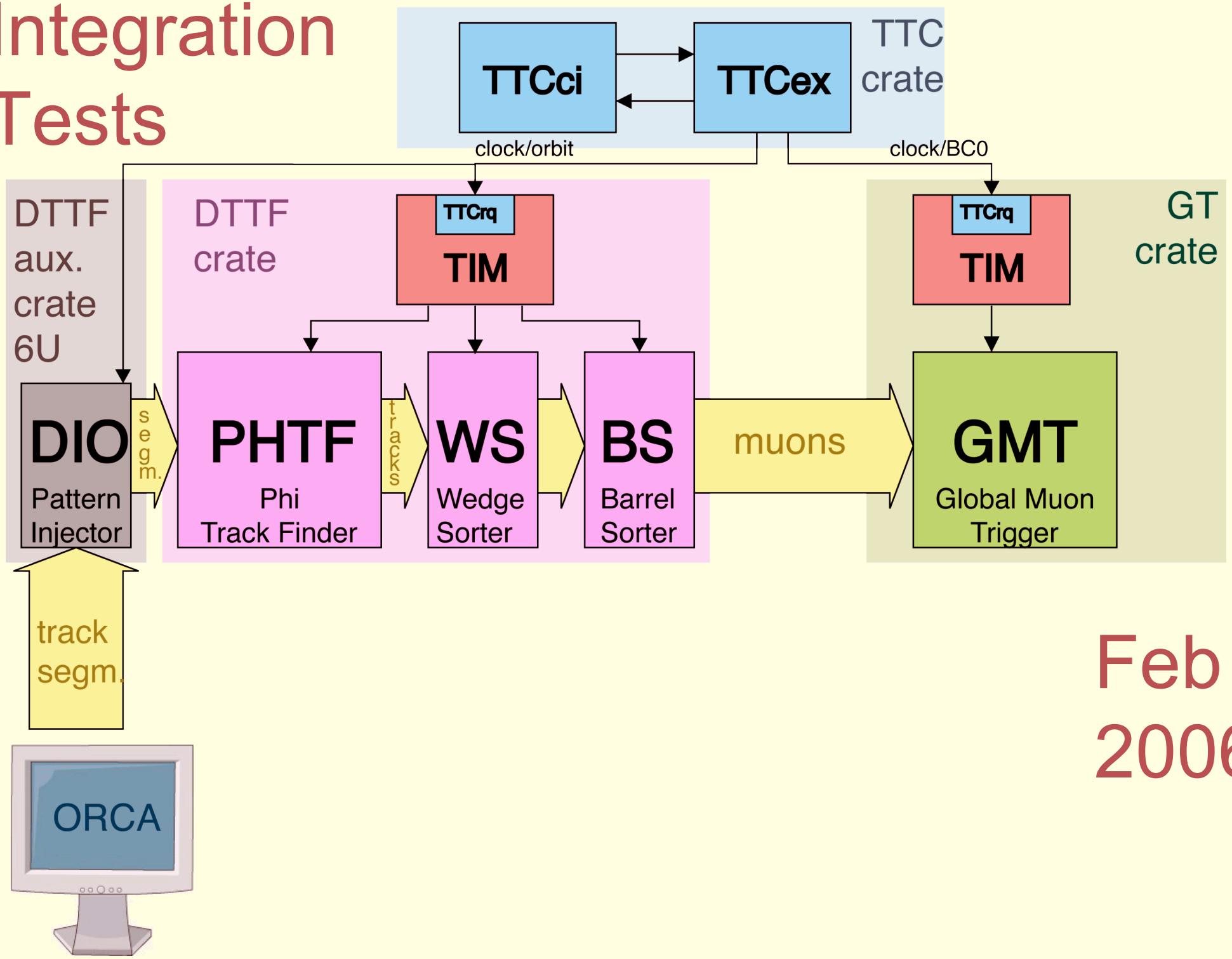
Jan 2006

Integration Tests



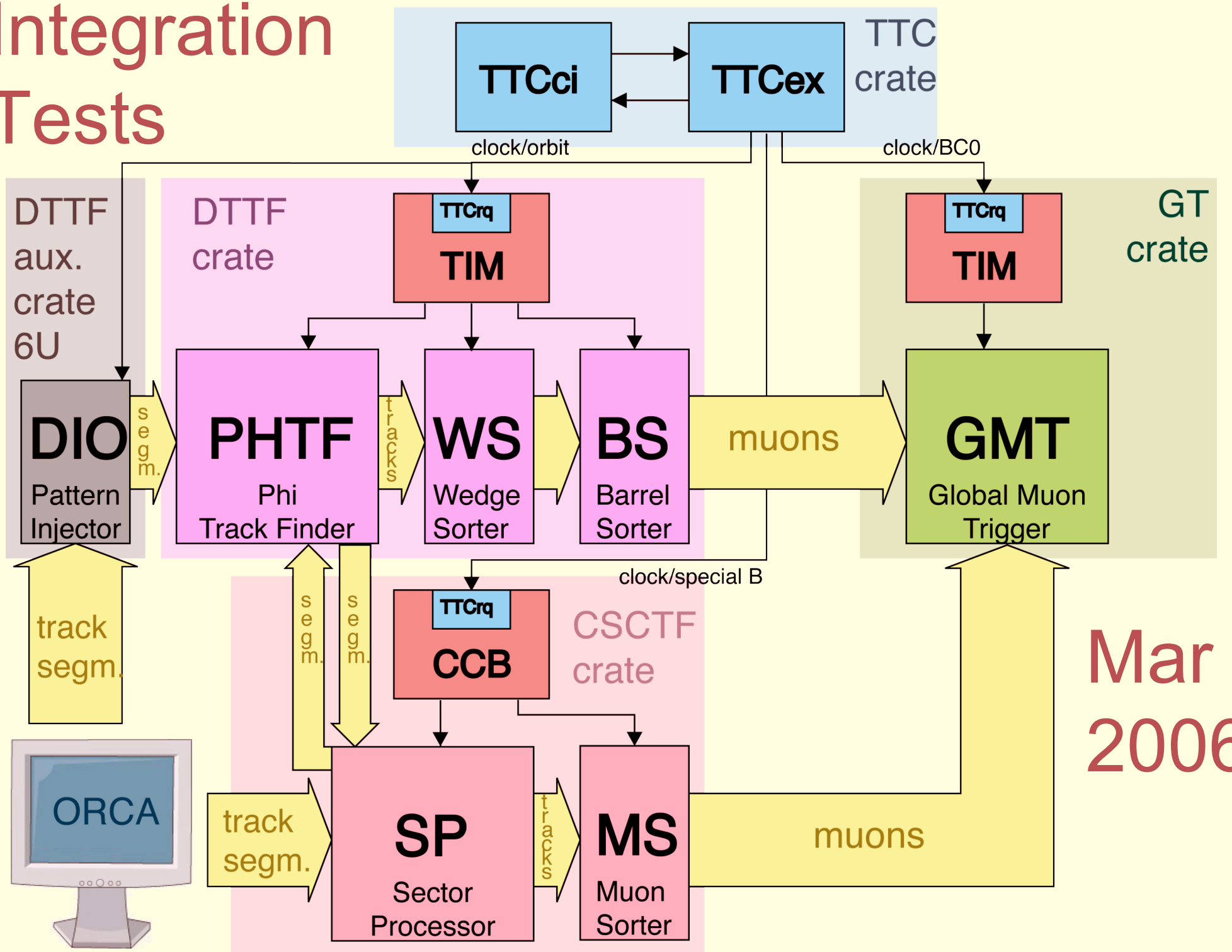
Jan 2006

Integration Tests



Feb 2006

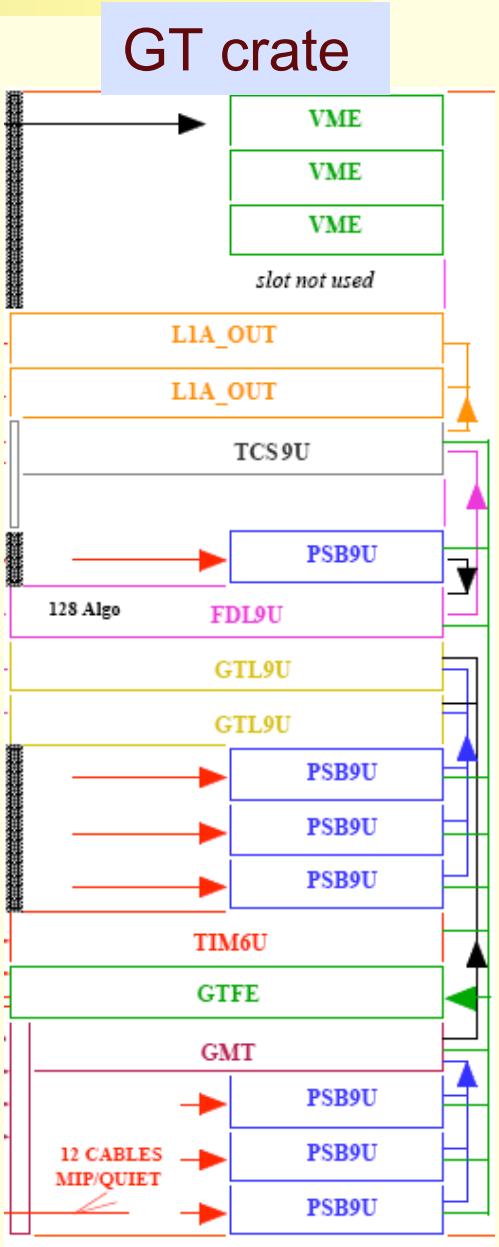
Integration Tests



Mar 2006

Tests with PSB

- Only one **PSB** board available at CERN for the moment (3 PSBs foreseen for the GMT input)
- In January, tests were done using special ORCA data. Tests revealed a few bit errors.
- In order to localise these errors, Tobias has written a test firmware incorporating spy memories at the GMT MIP/Quiet FPGA's. With this firmware the bit errors could be easily localised.
- Other PSB slots were tested. Identified a little mechanical problem with the last slot. New modified PSB module will be sent from Vienna.

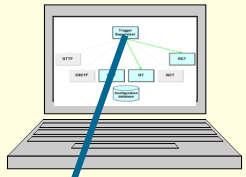


SW activities

- Configuration database is under preparation (see last meeting)
- On the fly development of test SW for the integration activities in b. 904 is ongoing
- Test firmware for MIP/Quiet FPGAs has been prepared and tested.
- New step in the integration with Trigger Supervisor:
  Tobias with Ildefons, Marc and Philipp have implemented the PSB-GMT test as a Trigger Supervisor operation with fake DTTF cell represented by the PSB board. This test was presented at the trigger integration meeting as a TS demonstration.

Philipp, HEPHY
Tobias, HEPHY
Marc, Wisconsin
Ildefons, HEPHY

Trigger Supervisor Application



ORACLE

cmsomds.cern.ch

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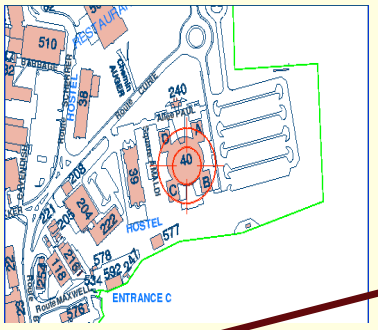
DSTORE



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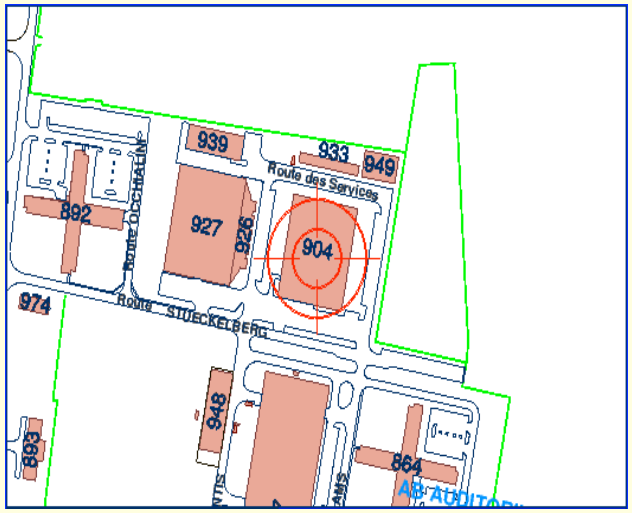
Central Cell

GT OSWI



Pcvahcms.cem.ch:3000

GT Cell

GT OSWI

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GMT Cell

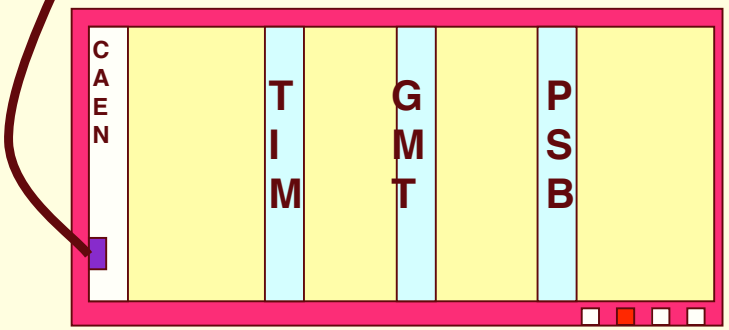
GMT OSWI

Pcvahcms.cem.ch:3002

"DTTF" Cell

GT OSWI

CAEN bus adapter driver



Global Trigger Crate

⇒ talk of Ildefons

Conclusions

- Individual connection tests with patterns from **DTTF** and **CSCTF** (Sorters) to **GMT** have been successfully completed in January.
- A more complicated test with **DTTF** involving **PHTF** using ORCA generated muons has revealed the importance of timing (5 modules in a chain). A few problems have been identified and will be further studied and corrected.
- A triangular test **DTTF-CSCTF-GMT** has started by setting up the timing. Test data based on ORCA simulations is under preparation.
- One of the successful tests (**PSB-GMT**) has been implemented in the Trigger Supervisor as an example procedure and used for demonstration.
- The integration with **RPC** will start next week