Integration tests with **G**lobal **M**uon **T**rigger

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CMS Trigger meeting
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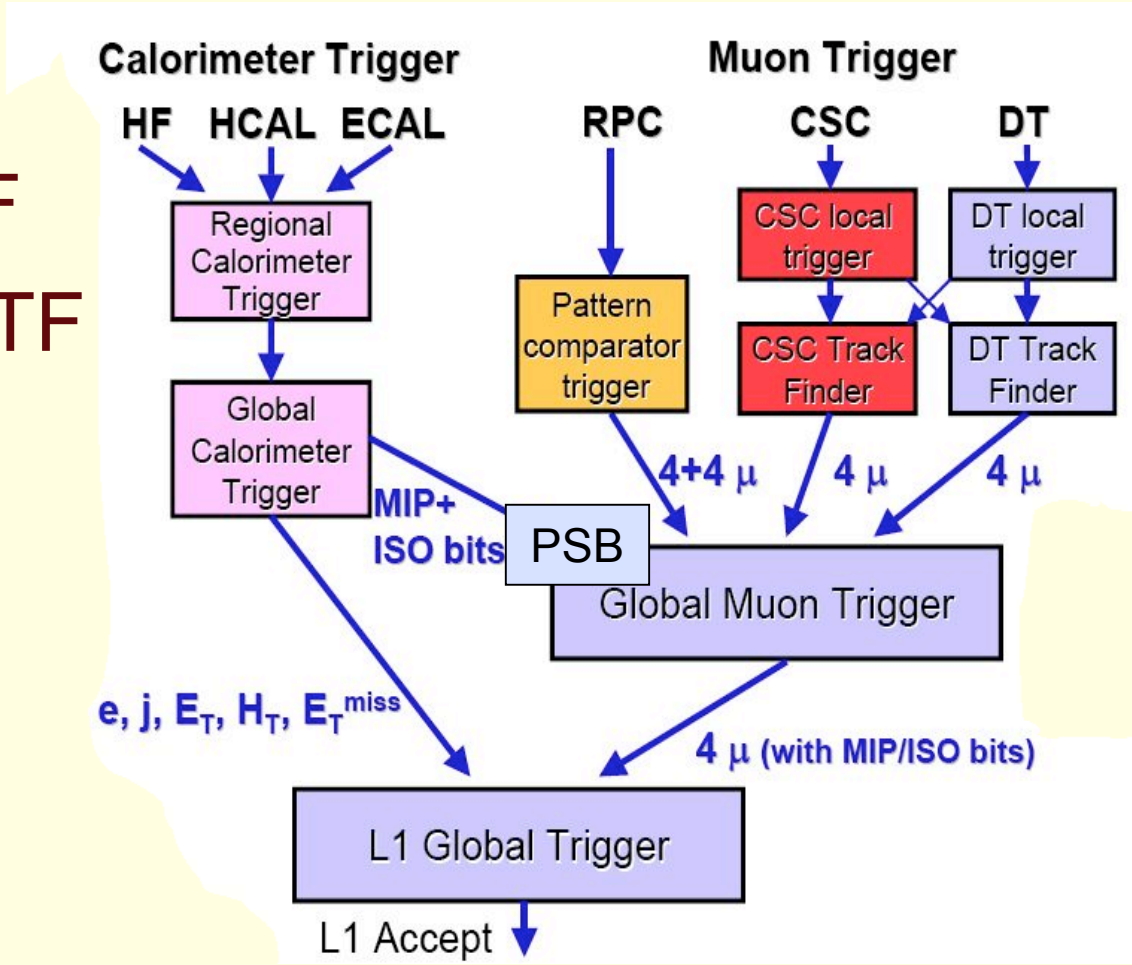
Overview

- GMT Self-tests
- GMT Integration tests
  - Test with PSB
  - Test with DTTF
  - Test with CSCTF
- SW activities
- Conclusions

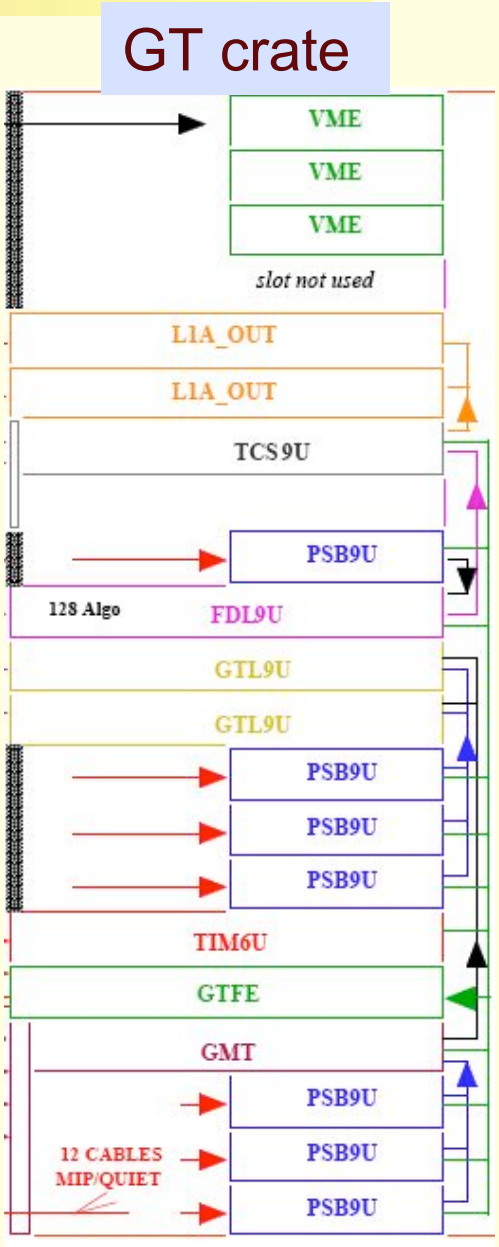


GMT Self-tests

- Self-tests of the GMT module were done in Vienna using ORCA data ($H \rightarrow ZZ \rightarrow 4\mu$)- full internal functionality reproduced (apart from 4 bit errors - 2 corrected in the firmware)
- Mid-December GMT module arrived at CERN
- Before Christmas self-tests were repeated in b. 904
- From the beginning of January GMT was **ready for integration**

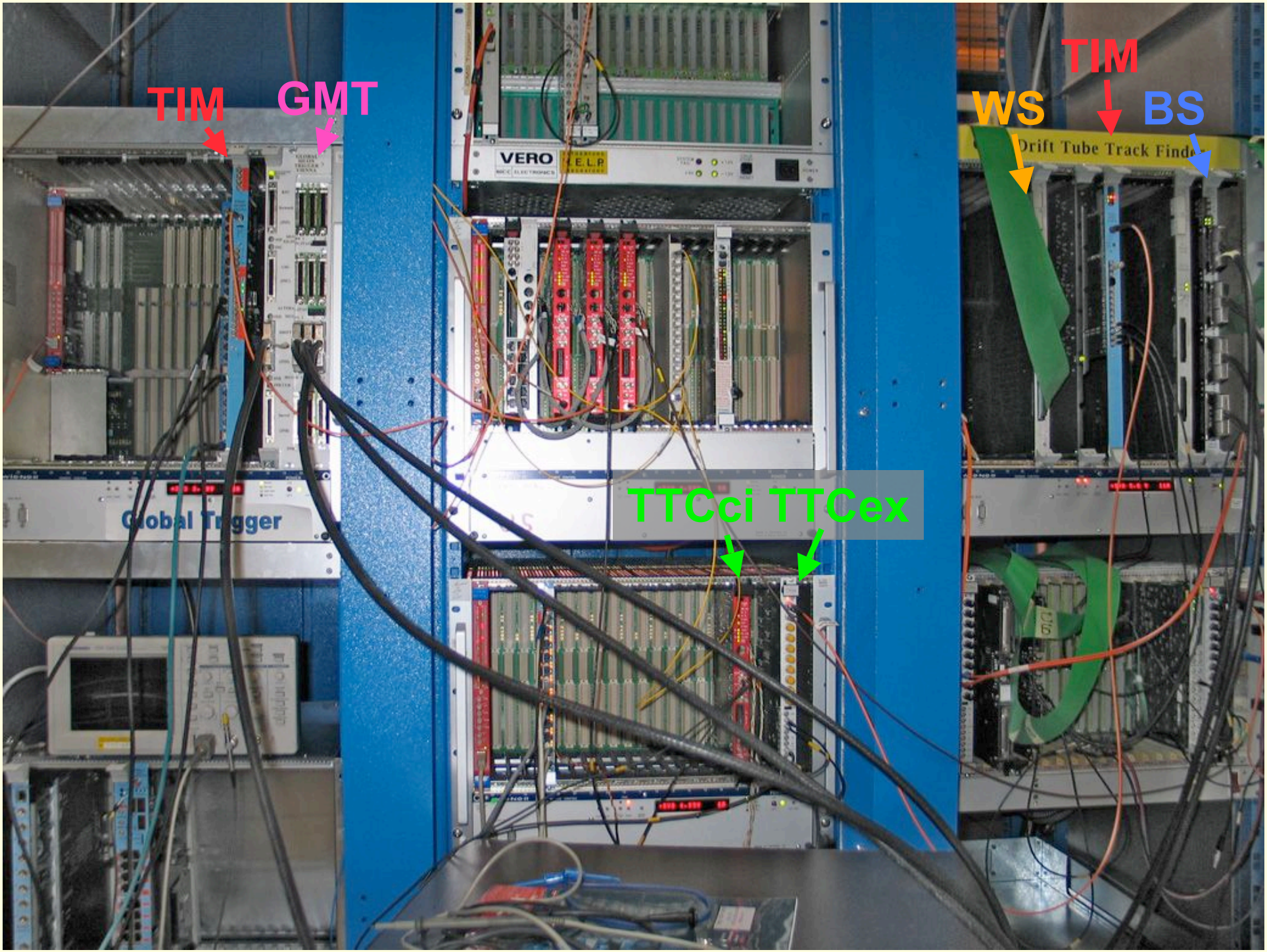
Test with PSB

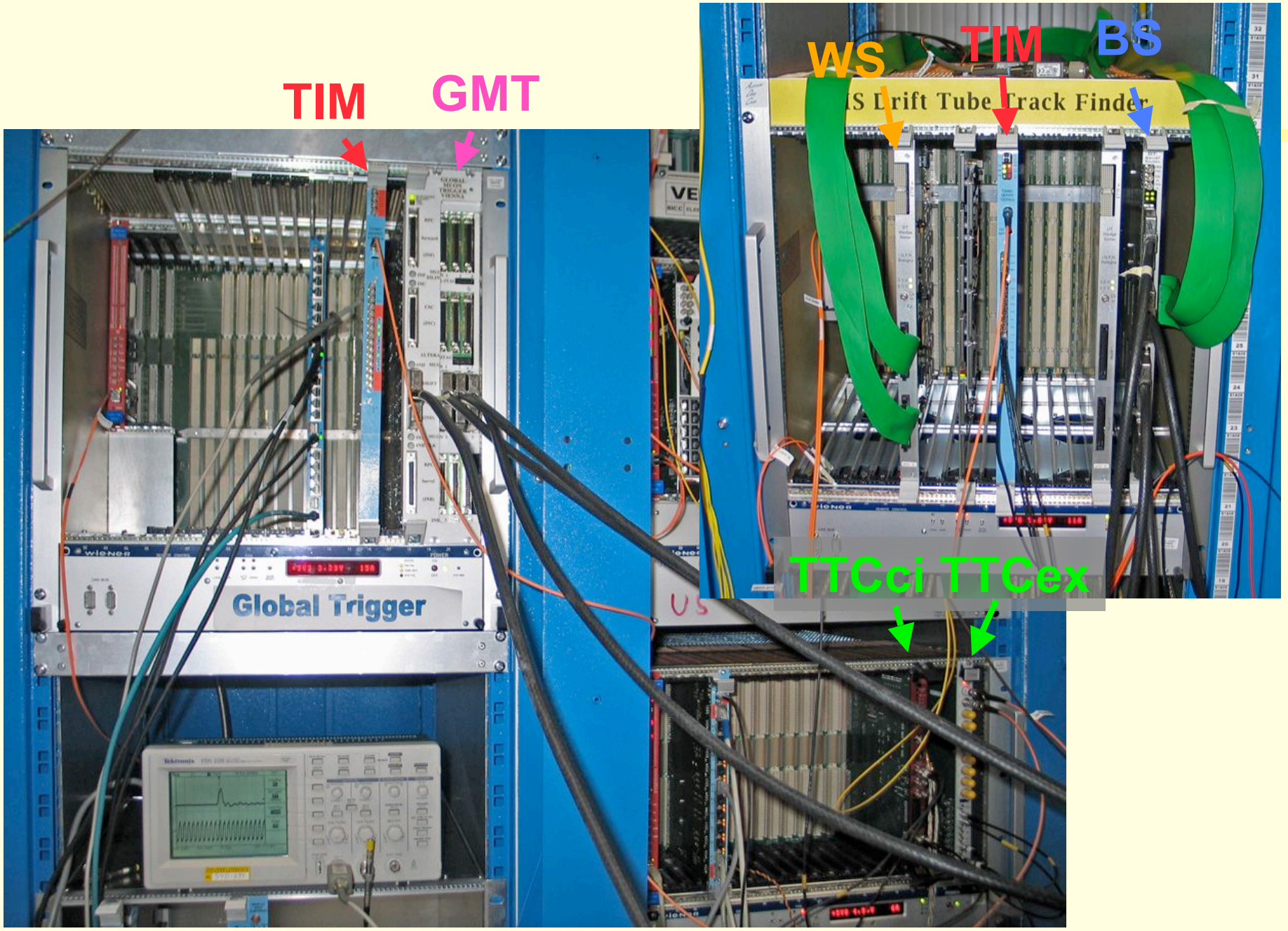
- **PSB** (**P**ipelined **S**ynchronising **B**uffer) synchronises the GCT inputs into GT and **GMT**
- Only one **PSB** board available at CERN for the moment (3 PSBs foreseen for the GMT input)
- Test was done using special ORCA data:
  - modified to account for one PSB only
  - MIP/ISO information written into the PSB board
  - Muon inputs written into GMT simulation memories in the input FPGA's
  - Timing (clock and BCreset) provided by the GT **TIM** module
- After a fine timing adjustment, data were received and combined by the **GMT** correctly
- A couple of transmission bit errors found
- **Tobias** is preparing new test firmware to localise these bit errors



Test with DTTF

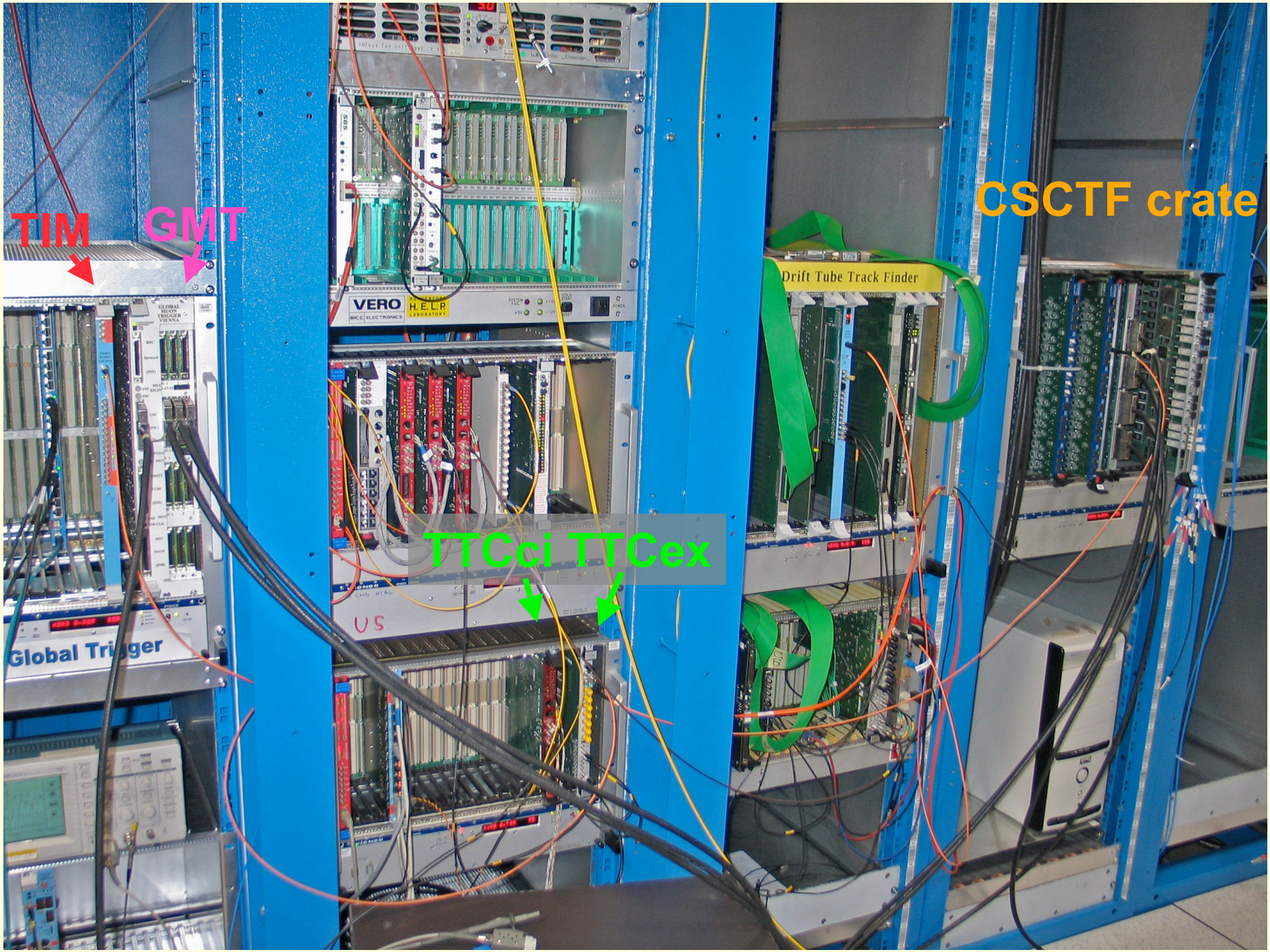
- In collaboration with **Janos**
- Bit patterns sent from **Wedge Sorter** (WS) through **Barrel Sorter** (BS) into **GMT**
- Common clock provided by **TTCci** and split by **TTCex** (thanks to **Jan** for his assistance) and received by **TIM** modules in both crates
- All 16 **GMT** input connectors were scanned (4 bit errors in total found on the GMT side)
- Next step is to try to connect more modules in a chain and use ORCA data

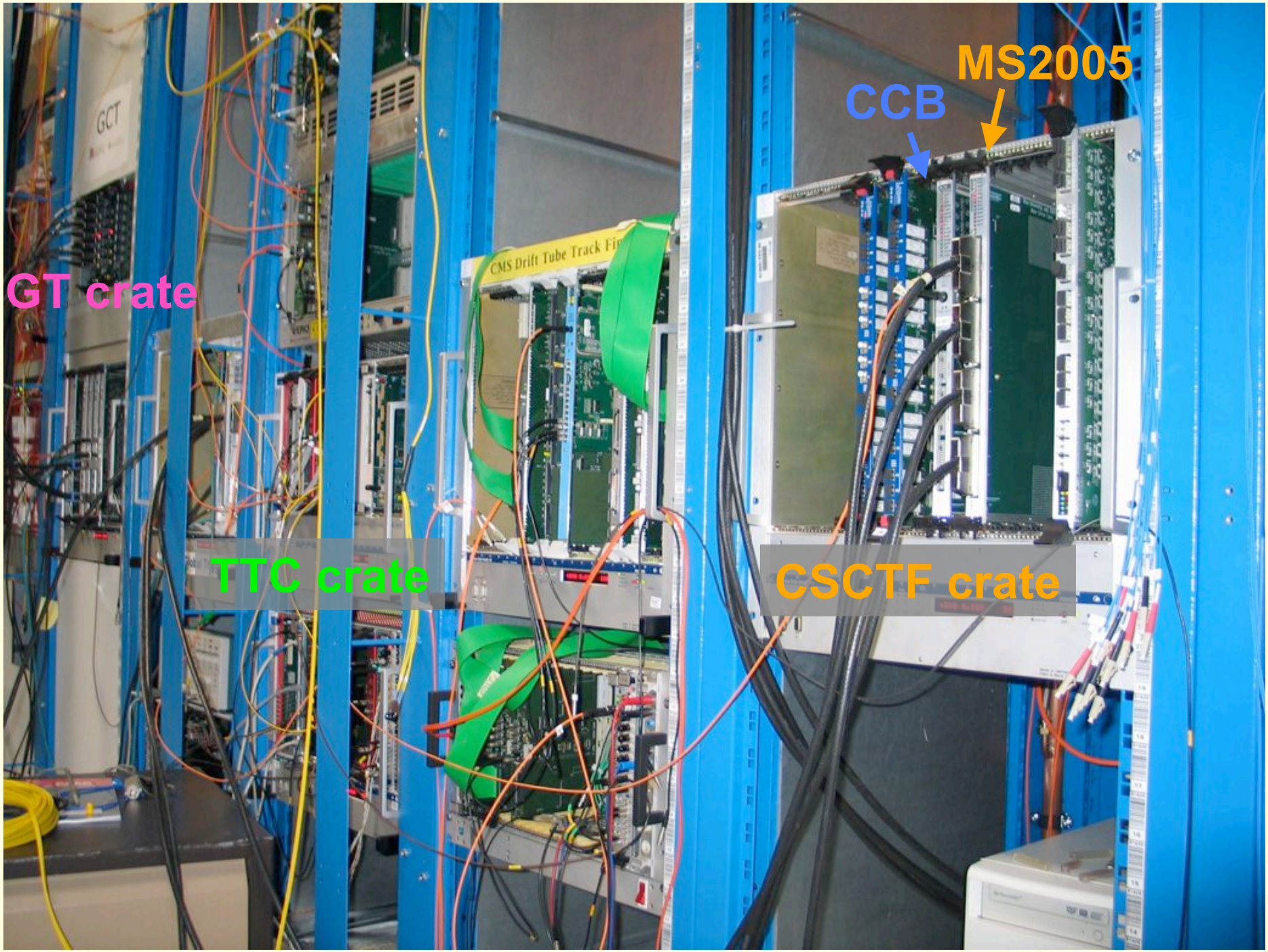

TIM
GMT
TIM
WS
BS
VERO
Global Trigger
TTCci TTCex


TIM
GMT
Global Trigger
WS
TIM
BS
TTCci TTCex

Test with CSCTF

- Mid-January the new **CSC Muon Sorter** board (MS2005) arrived at CERN
- **Dan** installed it in the CSCTF crate
- It was self-tested remotely by **Sang-Joon Lee** from Rice
- Our interconnection test was synchronised using **TTCci/TTCex** system connected to **TIM** board in the GT crate and **CCB** (Clock and Control Board) in the CSCTF crate:
  - Test pattern was written into MS RAMs
  - The transmission was triggered by a BC0 broadcast from TTCci
  - The same signal triggered reading of spy memories in the **GMT** input FPGA
  - Data were aligned for comparison with appropriate delay
- No problems have been found


TIM
GMT
CSCTF crate
TTCci TTCex
Drift Tube Track Finder
VERO
H.E.L.P
Global Trigger

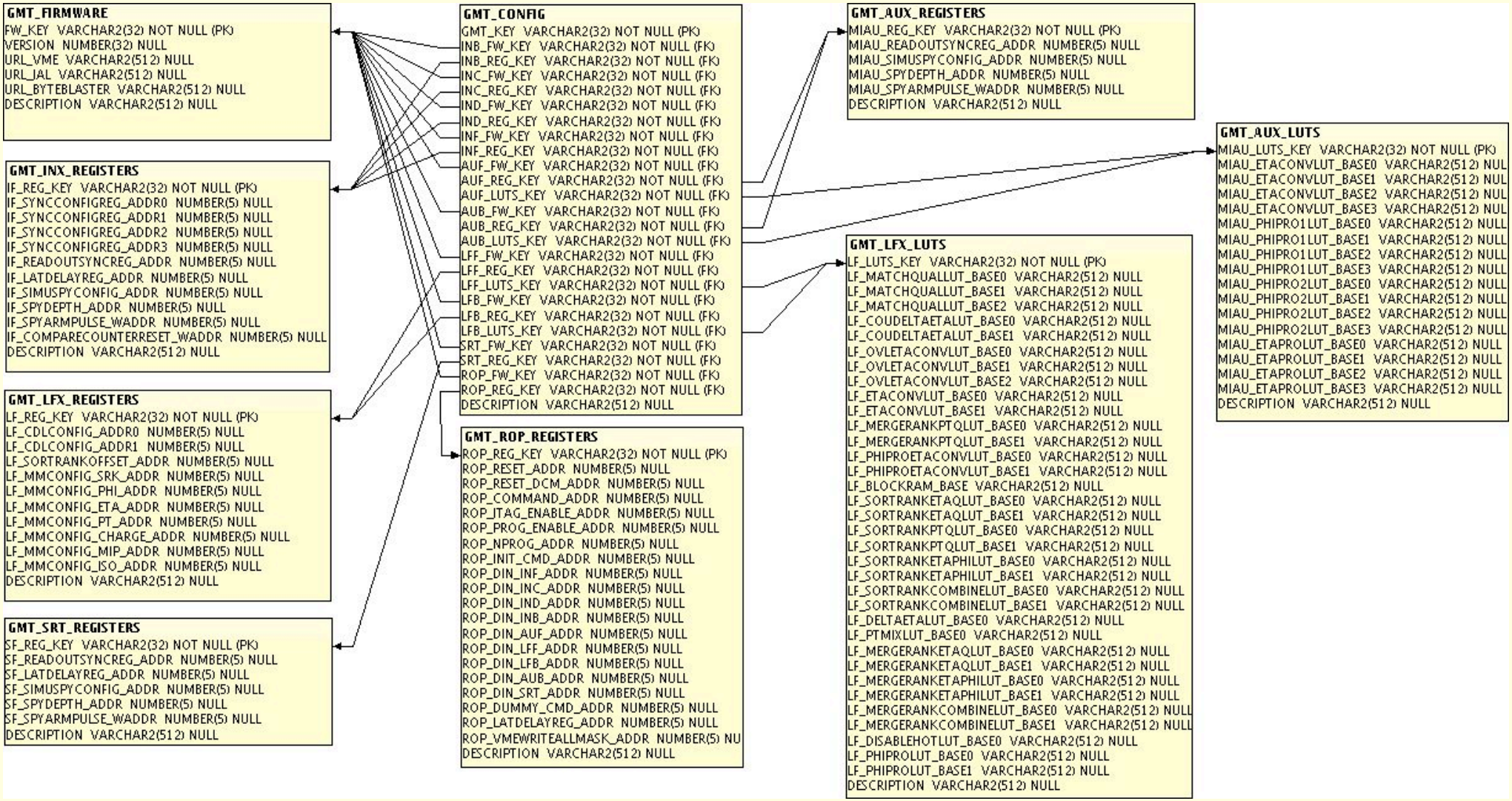

MS2005
CCB
GT crate
TTC crate
CSCTF crate


GCT

SW activities

- On the fly development of test SW for the integration activities in b. 904
- New firmware with updated LUTs
- Test firmware for MIP/ISO FPGas
- Integration to Trigger Supervisor
- Configuration database

Layout of the GMT config. db



Conclusions

- Integration tests of several trigger chains leading to the **GMT** have been started in parallel in the integration area of b. 904
- **TTCci/TTCex** system has been installed and tested in the integration area as a basic synchronisation tool for these tests
- The **RPC** chain can be tested as soon as RPC electronics is ready (end of February?)
- Tests with **DTTF** and **CSCTF** will continue by adding new elements to the chain and using ORCA simulation to calculate the expected response