Global Muon Trigger and Global Trigger Software Review

Vienna Group:

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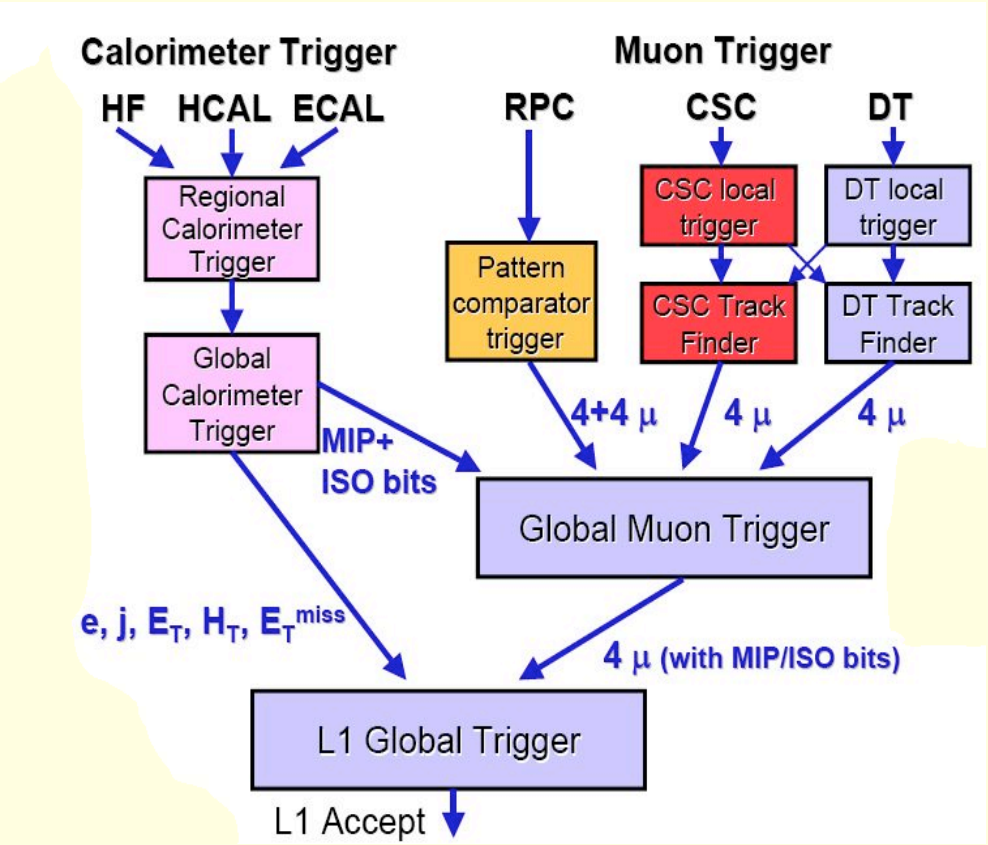
HEPHY Vienna

Trigger SW Review

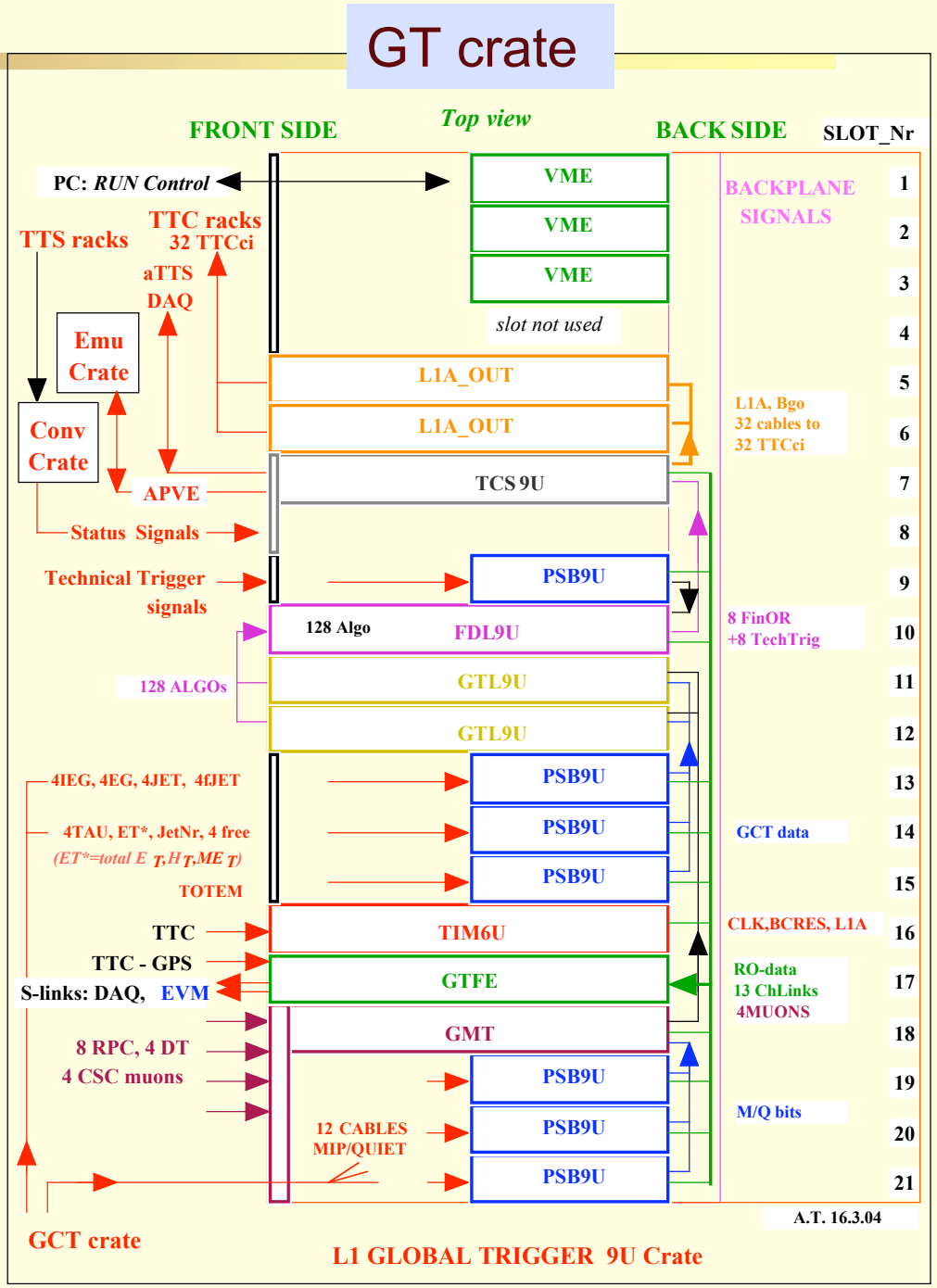
10 April 2006

Introduction



GMT/GT system is implemented in a single 9U VME crate (9 different VME modules)

GT crate



Firmware

GMT firmware

- fully implemented
- contains test features allowing loading and reading patterns at the inputs and outputs and real time bit error counting
- optional test firmware has been developed to add debugging power for calorimeter inputs

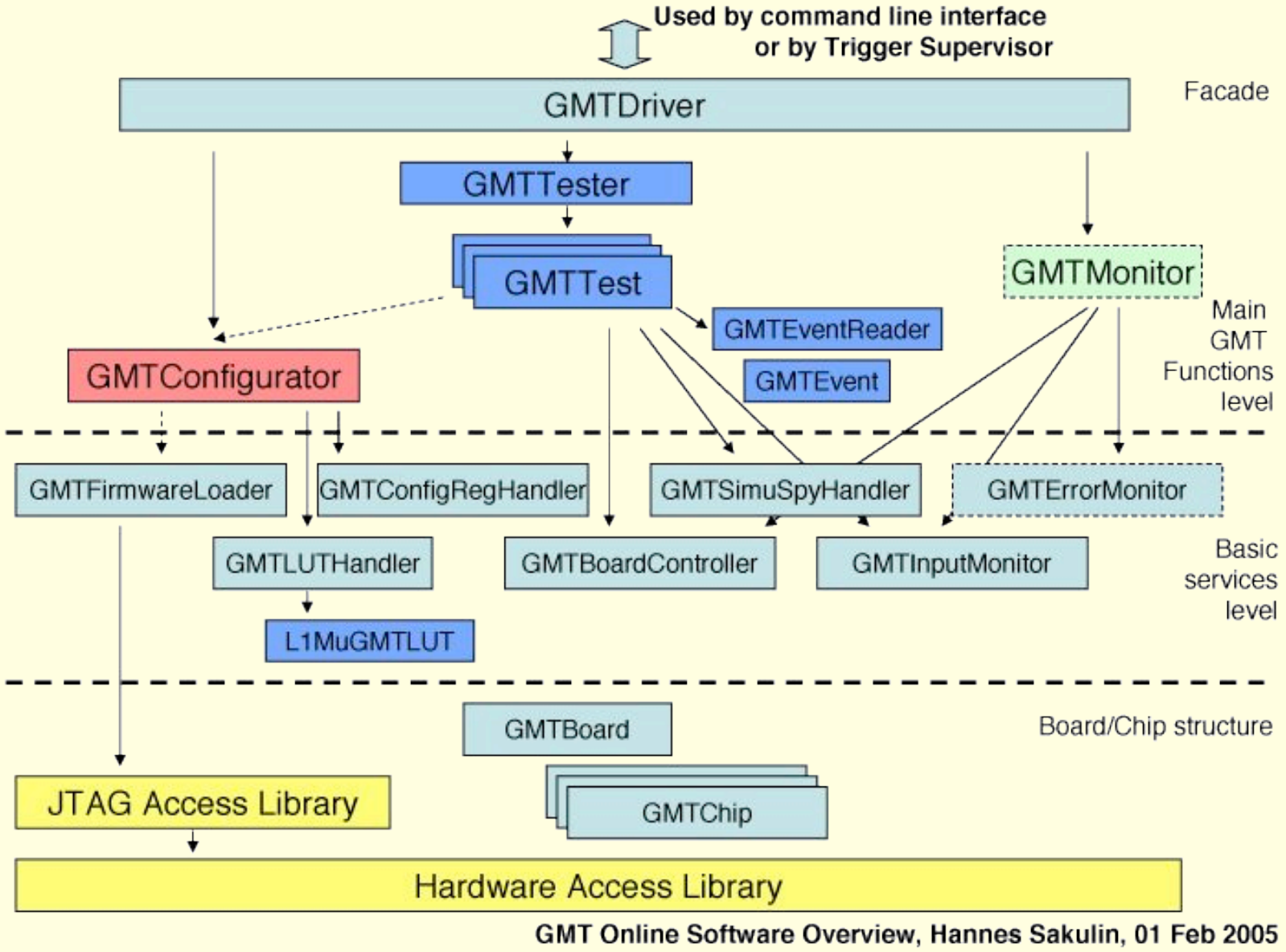
GT firmware

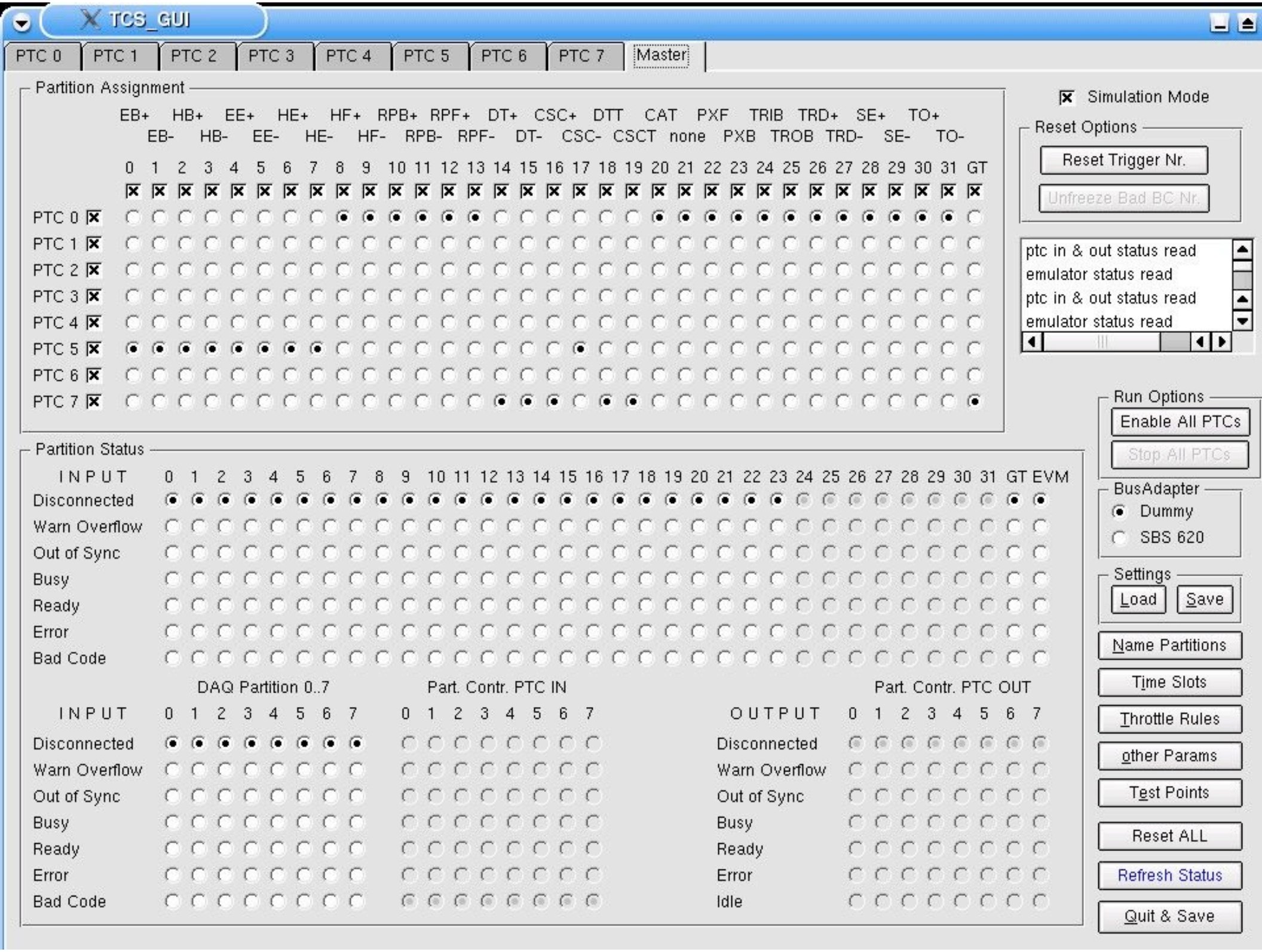
- full trigger functionality implemented
- a standalone program exists to translate XML files containing conditions and algorithms into VHDL code which can be precompiled and stored in the database
- some test and monitoring features still being developed
- modifications needed to prepare for the absence of GCT at the beginning of data taking

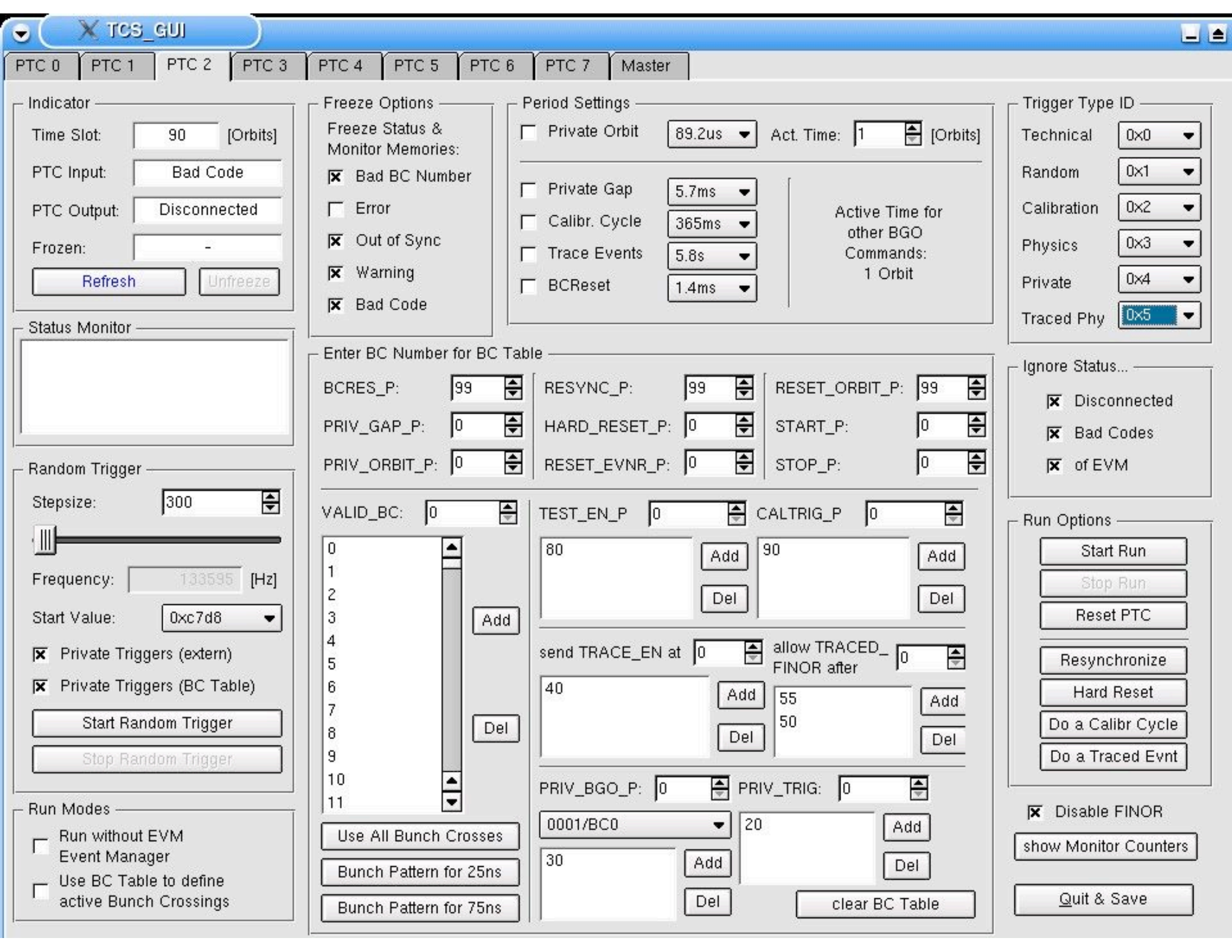
HW control

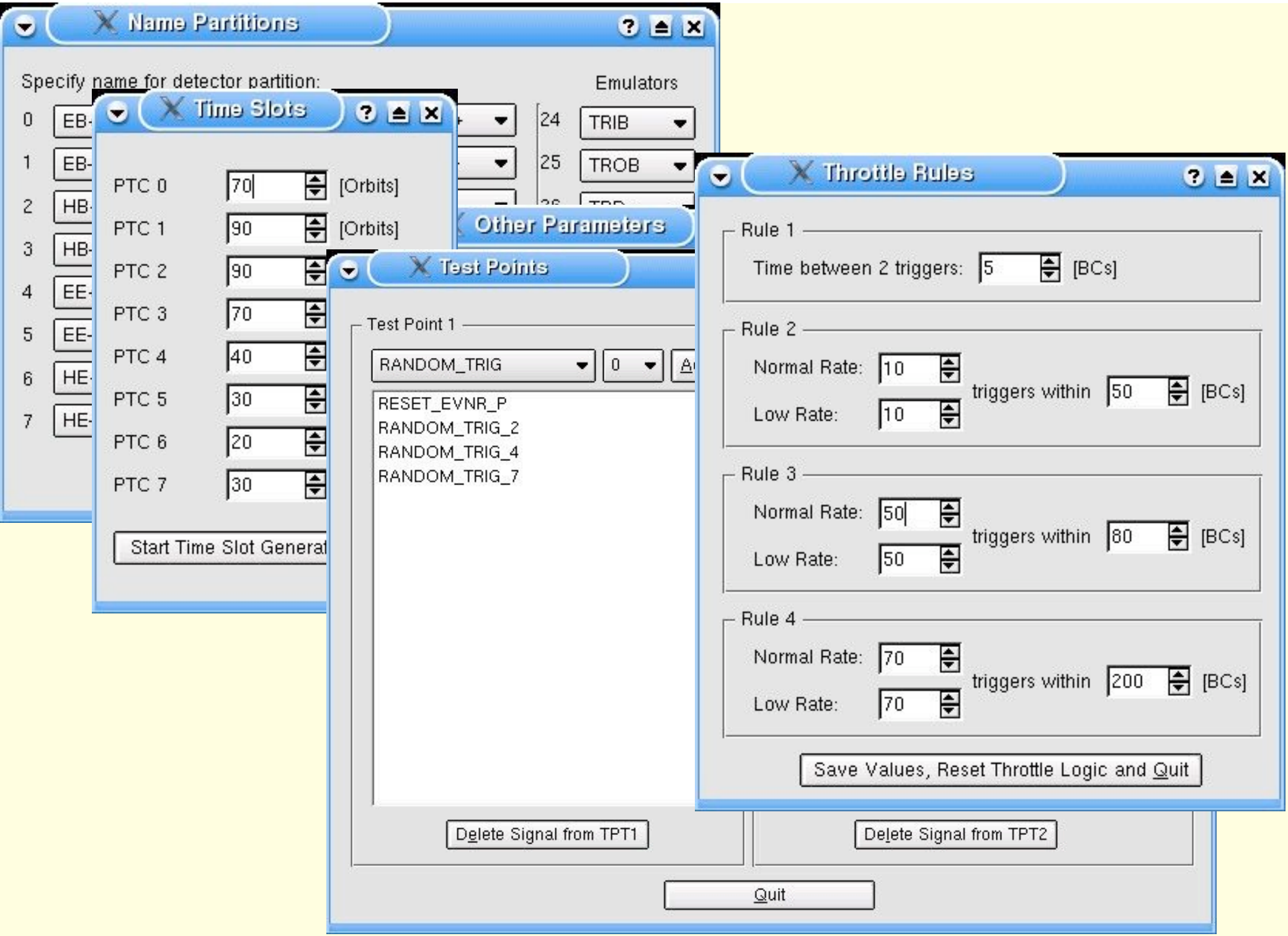
- **Command line programs** exist which allow full control of each board standalone. They contain also modules to perform individual tests which are being improved and added along with integration activities in b. 904.
- **Graphical user interfaces** are available for some of the modules. They are based on the same class libraries.
- These programs are successfully being used in the **interconnection tests in b. 904**. Most input connections were tested (DTTF-GMT, CSCTF-GMT, RPC-GMT, G(R)CT-GT,RPC-GT) using pattern transmission and reading and partially also ORCA-generated muons. No particular problems observed.

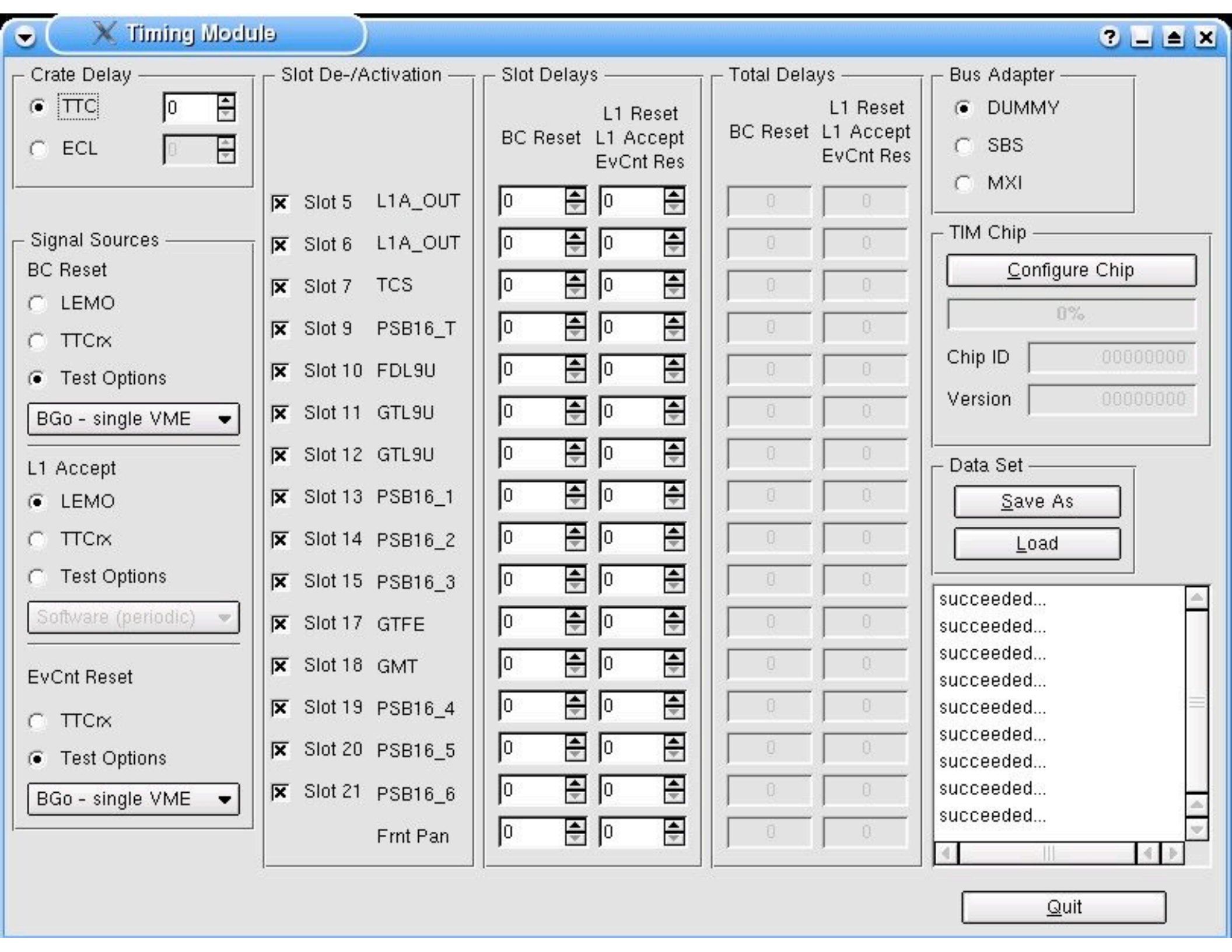
GMT online SW scheme

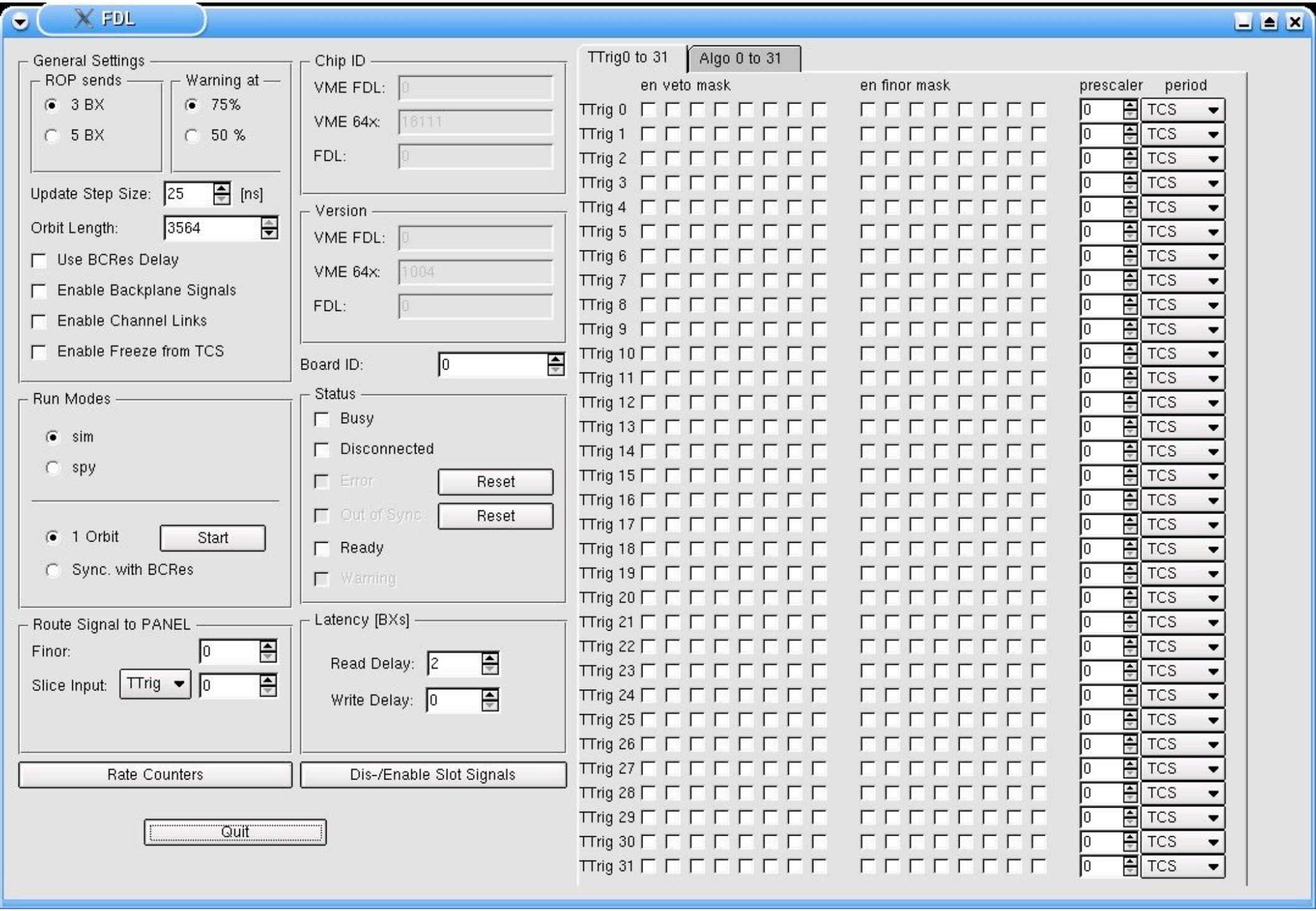



TCS_GUI
PTC 0
PTC 1
PTC 2
PTC 3
PTC 4
PTC 5
PTC 6
PTC 7
Master
Partition Assignment
EB+ HB+ EE+ HE+ HF+ RPB+ RPF+ DT+ CSC+ DTT CAT PXF TRIB TRD+ SE+ TO+
EB- HB- EE- HE- HF- RPB- RPF- DT- CSC- CSCT none PXB TROB TRD- SE- TO-
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 GT
PTC 0
PTC 1
PTC 2
PTC 3
PTC 4
PTC 5
PTC 6
PTC 7
Simulation Mode
Reset Options
Reset Trigger Nr.
Unfreeze Bad BC Nr.
ptc in & out status read
emulator status read
ptc in & out status read
emulator status read
Run Options
Enable All PTCs
Stop All PTCs
BusAdapter
Dummy
SBS 620
Settings
Load
Save
Name Partitions
Time Slots
Throttle Rules
other Params
Test Points
Reset ALL
Refresh Status
Quit & Save
Partition Status
INPUT 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 GT EVM
Disconnected
Warn Overflow
Out of Sync
Busy
Ready
Error
Bad Code
DAQ Partition 0..7
Part. Contr. PTC IN
Part. Contr. PTC OUT
INPUT 0 1 2 3 4 5 6 7
OUTPUT 0 1 2 3 4 5 6 7
Disconnected
Warn Overflow
Out of Sync
Busy
Ready
Error
Bad Code
Idle


TCS_GUI
PTC 0
PTC 1
PTC 2
PTC 3
PTC 4
PTC 5
PTC 6
PTC 7
Master
Indicator
Time Slot: 90 [Orbits]
PTC Input: Bad Code
PTC Output: Disconnected
Frozen: -
Refresh
Unfreeze
Status Monitor
Random Trigger
Stepsize: 300
Frequency: 133595 [Hz]
Start Value: 0xc7d8
Private Triggers (extern)
Private Triggers (BC Table)
Start Random Trigger
Stop Random Trigger
Run Modes
Run without EVM Event Manager
Use BC Table to define active Bunch Crossings
Freeze Options
Freeze Status & Monitor Memories:
Bad BC Number
Error
Out of Sync
Warning
Bad Code
Period Settings
Private Orbit 89.2us Act. Time: 1 [Orbits]
Private Gap 5.7ms
Calibr. Cycle 365ms
Trace Events 5.8s
BCReset 1.4ms
Active Time for other BGO Commands: 1 Orbit
Enter BC Number for BC Table
BCRES_P: 99
RESYNC_P: 99
RESET_ORBIT_P: 99
PRIV_GAP_P: 0
HARD_RESET_P: 0
START_P: 0
PRIV_ORBIT_P: 0
RESET_EVNR_P: 0
STOP_P: 0
VALID_BC: 0
0 1 2 3 4 5 6 7 8 9 10 11
Add
Del
Use All Bunch Crosses
Bunch Pattern for 25ns
Bunch Pattern for 75ns
TEST_EN_P 0
CALTRIG_P 0
80
90
send TRACE_EN at 0
allow TRACED_ FINOR after 0
40
55
50
PRIV_BGO_P: 0
PRIV_TRIG: 0
0001/BC0
20
30
clear BC Table
Trigger Type ID
Technical 0x0
Random 0x1
Calibration 0x2
Physics 0x3
Private 0x4
Traced Phy 0x5
Ignore Status...
Disconnected
Bad Codes
of EVM
Run Options
Start Run
Stop Run
Reset PTC
Resynchronize
Hard Reset
Do a Calibr Cycle
Do a Traced Evnt
Disable FINOR
show Monitor Counters
Quit & Save


Name Partitions
Specify name for detector partition:
Emulators
0
1
2
3
4
5
6
7
24
25
TRIB
TROB
Time Slots
PTC 0
70
[Orbits]
PTC 1
90
[Orbits]
PTC 2
90
PTC 3
70
PTC 4
40
PTC 5
30
PTC 6
20
PTC 7
30
Start Time Slot Generat
Other Parameters
Test Points
Test Point 1
RANDOM_TRIG
0
RESET_EVNR_P
RANDOM_TRIG_2
RANDOM_TRIG_4
RANDOM_TRIG_7
Delete Signal from TPT1
Delete Signal from TPT2
Quit
Throttle Rules
Rule 1
Time between 2 triggers:
5
[BCs]
Rule 2
Normal Rate:
10
triggers within
50
[BCs]
Low Rate:
10
Rule 3
Normal Rate:
50
triggers within
80
[BCs]
Low Rate:
50
Rule 4
Normal Rate:
70
triggers within
200
[BCs]
Low Rate:
70
Save Values, Reset Throttle Logic and Quit


Timing Module
Crate Delay
TTC
0
ECL
Signal Sources
BC Reset
LEMO
TTCrx
Test Options
BGo - single VME
L1 Accept
LEMO
TTCrx
Test Options
Software (periodic)
EvCnt Reset
TTCrx
Test Options
BGo - single VME
Slot De-/Activation
Slot 5 L1A_OUT
Slot 6 L1A_OUT
Slot 7 TCS
Slot 9 PSB16_T
Slot 10 FDL9U
Slot 11 GTL9U
Slot 12 GTL9U
Slot 13 PSB16_1
Slot 14 PSB16_2
Slot 15 PSB16_3
Slot 17 GTFE
Slot 18 GMT
Slot 19 PSB16_4
Slot 20 PSB16_5
Slot 21 PSB16_6
Frnt Pan
Slot Delays
BC Reset
L1 Reset L1 Accept EvCnt Res
Total Delays
BC Reset
L1 Reset L1 Accept EvCnt Res
Bus Adapter
DUMMY
SBS
MXI
TIM Chip
Configure Chip
0%
Chip ID
00000000
Version
00000000
Data Set
Save As
Load
succeeded...
succeeded...
succeeded...
succeeded...
succeeded...
succeeded...
succeeded...
succeeded...
succeeded...
Quit


FDL
General Settings
ROP sends
3 BX
5 BX
Warning at
75%
50 %
Update Step Size: 25 [ns]
Orbit Length: 3564
Use BCRes Delay
Enable Backplane Signals
Enable Channel Links
Enable Freeze from TCS
Chip ID
VME FDL: 0
VME 64x: 16111
FDL: 0
Version
VME FDL: 0
VME 64x: 1004
FDL: 0
Board ID: 0
Run Modes
sim
spy
1 Orbit
Start
Sync. with BCRes
Status
Busy
Disconnected
Error
Reset
Out of Sync
Reset
Ready
Warning
Route Signal to PANEL
Finor: 0
Slice Input: TTrig 0
Latency [BXs]
Read Delay: 2
Write Delay: 0
Rate Counters
Dis-/Enable Slot Signals
Quit
TTrig0 to 31
Algo 0 to 31
en veto mask
en finor mask
prescaler
period
TTrig 0
TTrig 1
TTrig 2
TTrig 3
TTrig 4
TTrig 5
TTrig 6
TTrig 7
TTrig 8
TTrig 9
TTrig 10
TTrig 11
TTrig 12
TTrig 13
TTrig 14
TTrig 15
TTrig 16
TTrig 17
TTrig 18
TTrig 19
TTrig 20
TTrig 21
TTrig 22
TTrig 23
TTrig 24
TTrig 25
TTrig 26
TTrig 27
TTrig 28
TTrig 29
TTrig 30
TTrig 31
TCS

Integration with Trigger Supervisor

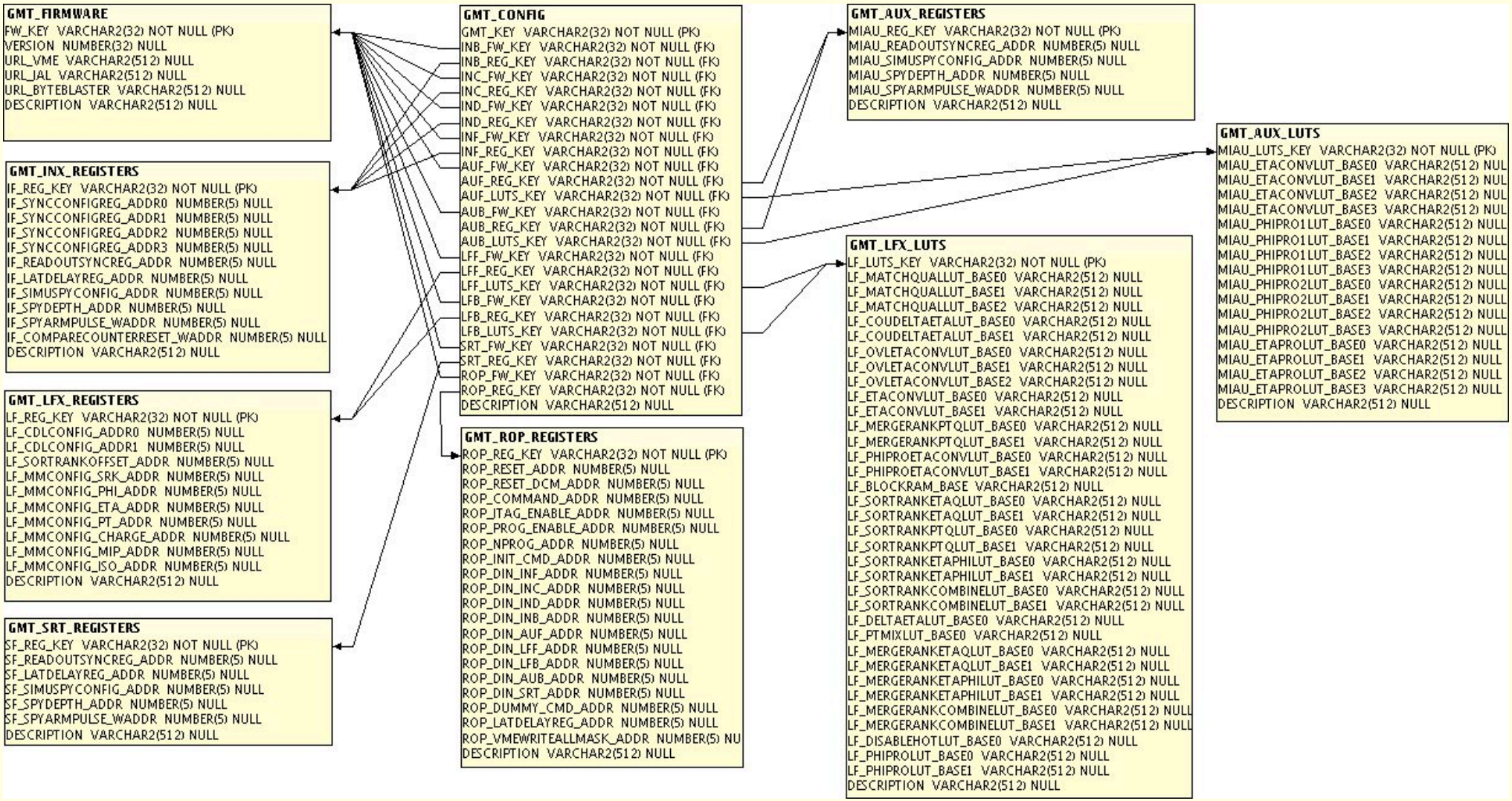
DATABASES:

- connection using DStore tested
- schemes for GMT, TCS, PSB, TIM
- could start with population

OPERATIONS:

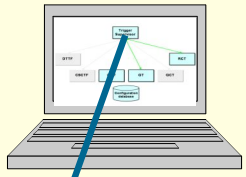
- standard operations implemented and tested
- one interconnection test PSB/GMT implemented
- one interconnection test GMT/GTL in progress

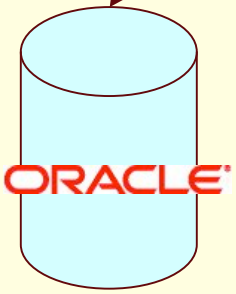
Layout of the GMT config. db



Philipp, HEPHY
Tobias, HEPHY
Marc, Wisconsin
Ildefons, HEPHY

Trigger Supervisor application

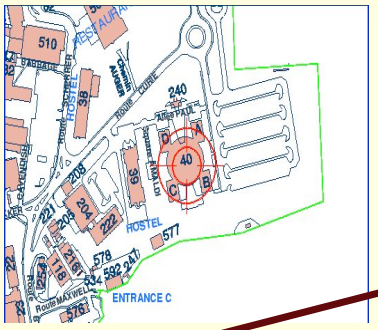




cmsomds.cern.ch

gtswpc2.cem.ch:1972

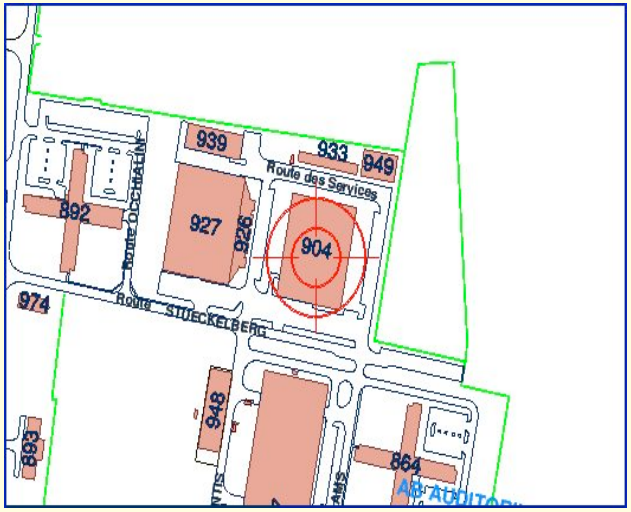
DSTORE



gtswpc1.cem.ch:1972

Central Cell

GT OSWI



Pcvahcms.cem.ch:3000

GT Cell

GT OSWI

Pcvahcms.cem.ch:3001

GMT Cell

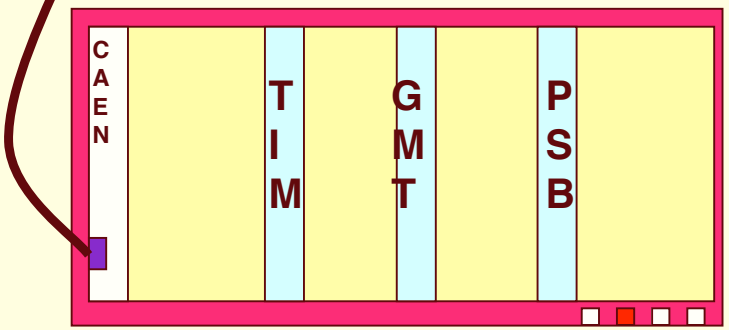
GMT OSWI

Pcvahcms.cem.ch:3002

"DTTF" Cell

GT OSWI

CAEN bus adapter driver



Global Trigger Crate

Integration with Trigger Supervisor

COMMANDS:

- commands implemented for TCS, PSB, TIM, FDL, GMT
- TCS commands offer 80% of the functionality of the standalone GUIs
- 50 % of the TCS commands tested successfully
- possible to control individual DAQ-PTC
- TIM commands allow setup of TIM for interconnection tests
- FDL commands allow readout of rate counters and setup of prescalers
- PSB commands allow simple tests

USER INTERFACE:

- GT and GMT are using the generic Trigger Supervisor GUI
- A framework for implementing standalone GUIs in the Trigger Supervisor under development

at least 2 students continuously working on this

GMT simulation/emulation

- **Production version in ORCA**
  - **used e.g. for calculation of L1 muon trigger performance in PTDR.**
  - **fully compatible with hardware**
  - **used to produce GMT LUTs,**
  - **results from ORCA were tested to be identical to hardware results (apart from few bit errors) - actually used to test hardware**
- **New private standalone version available in ORCA framework**
  - **Used to emulate GMT logic with different configurations using same input data/patterns as used for hardware tests.**

This standalone version will be used as a starting point for the migration to CMSSW.

GT simulation/emulation

PRODUCTION VERSION in ORCA

- **only simple conditions (thresholds) and algorithms (trigger Menu)**
- **trigger steering data input in ASCII files provided by setup program**
- **trigger files are in ORCA /Data/L1GlobalTrigger/ for high/low Luminosity**
- **NOT COMPATIBLE with steering of Global Trigger Hardware**
- **software results from ORCA checked vs HARDWARE Simulation**
- **not with full capability of designed GLOBAL TRIGGER HARDWARE**
- **not full HARDWARE 'BIT' compatibility**

BASIC Components

Trigger Config	Trigger menu SETUP
PSB	PipeLineSynchronizing Buffer
	(Trigger Data from Calo's)
GTL	Global Trigger Logic
	Trigger Data from MUONS
	Trigger Logic / Menu/ Algorithms Calculation
FDL	Final Decision Logic

GT simulation/emulation

NEW GROUP-INTERNAL ORCA COMPATIBLE SOFTWARE

- **with full functionality of Global Trigger HARDWARE**
  for complicated ALGORITHMS
  2 muon Thresholds(isolated/non isolated / mip/iso bit check
- **advanced HARDWARE 'BIT' compatibility**
- **triggering/steering data in XML FORMAT, usable also for HARDWARE steering**
- **Graphical User Interface for XML setup**
- **values in XML file hexadecimal**
- **setup for 6U version/ 9U to be done ..**

This version will be used as a basis for the migration to CMSSW (Vasile Ghete)

The interface to the CMSSW EDM can be developed in a GT-GMT common effort.

Conclusions

- **GT/GMT firmware is fully operational. Only small changes needed for test/monitoring purposes.**
- **Class libraries for HW control exist with standalone, either command line or graphical, interfaces. Test modules are added along with HW integration tests.**
- **Interconnection tests in b. 904 up to now did not reveal any particular problem.**
- **Integration with Trigger Supervisor is continuing. Participating in preparation of the TS demonstrator at Cosmic Challenge. Tight on manpower (not a financial problem). Additional students will be hired.**
- **Simulation/emulation of GMT and GT is implemented in ORCA. Migration to CMSSW is starting. Should be ready until August.**