Timing Module

in the Level 1 Global Trigger

6U-Version

H. Bergauer, K. Kastner, M. Padrta, A. Taurok

Aug-05

Version To be updated for version V2

1 Abstract

Preliminary!!!

The TIM module contains the TTCrx chip that receives the common CMS timing and synchronization signals. A programmable TIM chip distributes the central 40 MHz clock, the common synchronization signals and the L1Accept signal to all modules in the GT (= Global Trigger) or DTTF (=Drift Tube Track Finder) crate. The TIM chip can simulate all TTC signals to run the GT crate during tests in stand-alone mode. Optionally for the Global Trigger crate the TIM chip contains memories to monitor input signals and a Readout Processor to append the monitored data bits to the GT events.

2 Design-questions

- There are no net-rules defined yet. The graphic implementation of the rules should take place on sheet 2 of top-of-hierarchy schematics.

- Ich weiß noch nicht, wie wir die Längenunterschiede von ca 1.5-2cm zw. den verschiedenen Backplane Signalen definieren sollen. (L1A, RESET, BCRES,CLK)
- Länge Clock signale
- FAST SIGNAL are to be defined!!!
- RESET_TIM from VME chip??? ==>yes SYSRES* from VMEbus???? ==>yes
- Serial R between LVCH16245 and TIM chip at external Lemo lines????
- Enable signals from TIM chip to RO_INTERFACE and LVDS_DRIVER changed!! See tim_check\tim_chip.xls

3 Logic description

3.1 Overview

3.2 TTCrx

TTCrx signals:

Clock: Clock 40, Clock 40Des1, Clock 40Des2;
Channel A: L1Accept Programmable *Delay in bx*
Channel B:
Broadcast Data Interface: Brcst[7:2], EvCntRes, BCntRes; BrcstStr1, BrcstStr2;
Data Interface: Dout[7:0], SubAddr[7:0], DQ[3:0], DoutStr
Counter Interface: BCnt[11:0], EvCntHStr, EvCntLStr, BCntStrb
Internal Registers:
BCcntr 12 bits, EvCntr 24 bit...reset by broadcast Reset
L1Acc:

3.3 Timing signals to back-plane and front panel

Programmable Delays

3.4 Reliability checks

Direct Connections to TCS……

3.5 Signal Emulation

3.6 L1A and readout of data

This chapter describes logic only used in the Global trigger crate. The functional simulation has not been done completely until now.

Started by a L1A request the Readout Processor (ROP) extracts data from the Ringbuffer memories. Then the data are sent over a multiplexer to the Channel Link chip to be transferred to the GTFE Readout board. The multiplexer accepts monitoring data on the other port and sends them every 2nd clock cycle also to via the Channel Link chip to the GTFE board. Event and monitoring data are flagged by the identifier word to check the transfer logic.

3.6.1 L1A QUEUE

The L1A queue is used to store incoming L1A signals in a FIFO. For every L1A data of a number of bunch crossings are extracted from the Ring Buffer.
A new L1A writes the first address of the data packet into a FIFO. This address is taken from a bunch crossing counter and the BCRES signal for this counter is delayed to consider the L1A latency.
The extraction logic fetches the first address from the FIFO and loads it into the RingBuffer Read-Address Counter. At the same time a Readout Length counter is updated from the RO_LENGTH register. Then one address after the other is applied to the Ring Buffer Dual Port Memory to extract all data words for the actual L1A. The contents are then stored in the derandomizing buffer. The logic extracts data until the RO-Length counter becomes =0. If there is still another L1A request pending the next start address is read from the FIFO and the procedure is repeated as described above.
A new L1A can write also a control bit into the FIFO. At the same time a 'Waiting Time' counter is started that runs until the control bit appears at the FIFO output port.
If the waiting time is longer then the time corresponding to 75% of the Ringbuffer a warning bit is set. If safety margin decreases to 1/16-th of the Ringbuffer then the error bit 'L1A_TOO_OLD' is set. A new L1A check can be done only if the previous check procedure has been finished.
An additional warning message will be sent if more then 63 L1As are pending.
In case of calibration event a second control bit is written with the L1A-start address into the FIFO.

3.6.2 RING BUFFER

The Ring Buffer Dual Port memories receive data continuously. A bunch crossing counter provides the write addresses. The reset signal for this address counter is delayed to consider the latency time of the input data. Therefore data of bunch crossing 'NN' are written into the address 'NN' modulo 1024. After 1024 clock cycles old data are overwritten.
As described above the extraction logic just applies addresses to the Ring buffer memories to extract data.
If enabled the content of the Ring buffer will be 'frozen' in case of an error. Also a VME-instruction can freeze the Ring Buffer immediately.

3.6.3 DERANDOMIZING BUFFER

The derandomizing buffer, called RO_BUF (=readout buffer) is implemented as FIFO. It receives the extracted data bits and identifier bits to flag calibration events.
An additional readout buffer receives the corresponding bunch crossing numbers also flagged by 2 bits.

DATA IDENTIFIER bits 17,16	
00	No data/ header words
01	event data
10	calibration event data
11	bunch crossing number

3.6.4 READOUT PROCESSOR

The Readout Processor (ROP) implemented as a state machine runs as long as there data waiting in the derandomizing buffers and as long as the GTFE board is ready to accept event data. The ROP creates event records consisting of an Identifier, Event Number, trigger data, Word Count and EOR. Between records its sends IDLE words via the Channel Link chips to the GTFE board.
First ROP broadcasts a common read instruction to all derandomizing buffers to move data bits of a bunch crossing into registers. Then it resets the Word Counter, sends the IDENTIFIER, the high Event Number bits and the low Event Number bits.
Now it collects one data word after the other from the registers. Then it broadcasts a new read signal to all derandomizing buffers to collect the data bits from the next bunch crossing. This is done until all data bits of an L1A are transferred.
The ROP appends then the Count and the EOR identifier to finish the event record.

3.6.5 Data format

Bits 15- 0: trigger data or BC numbers or identifiers, word count, idle-id
Bits 17-16: Data Identifier bits. *// See table above.*
Bits 19-18: 0 0
~~Bits 26-20: incrementing number~~
~~Bit 27: =0 EVENT data, =1 Monitoring data~~
Remark: This format has to be changed to get a 28 bit IDLE code. Not done in schematic.
Bits 25-20: incrementing number
Bit 27-26: =00 IDLE; =01 Event; =10 Monitoring; =11 xxx

3.7 Messages from TCS via TTC

3.8 Fast Signals to TCS

The TIM board sends the standard set of Fast Signals to the TCS board like all other GT boards.

ROBUF= Readout Buffer FIFO
RIBUF= RING BUFFER for data 1 kwords
L1A-Queue =FIFO to store new L1A

TIM_ERROR signals:
- BAD_MAX_BC *// BCR comes later than expected by the BC-counter*
- BAD_LOCAL_BC *// The TTC and local BC number do not agree.*
- DBERR *// Double bit error from the TTCrx chip*

TIM_OUT_OF_SYNC signals
- ROBUF_SYNCERR *// ROBUFs become not empty at the same time.*
- ROBUF_OVF *// Readout Buffer FIFO are full and a write access is pending.*
- L1A_TOO_OLD *// The L1A have to wait too long in the L1A queue. // Data in the RingBuffer might be overwritten.*
- TOO_MANY_L1A *// More than 63 L1As are waiting in the L1A queue.*

TIM_WARNING_OVFLO
- L1A_OLD_WARN *// More than 75% of the RingBuffer has been overwritten since the requested L1A data*
- WARNING_ROBUF_OVF *// The ROBUF FIFOs are 75% full.*

TIM_READY
- =TIM_SETUPDONE bit=1 and TTC_READY=1 and TIM_BUSY=0 *// The TIM board is ready to run.*

TIM_BUSY
- =TIM_SETUPDONE bit=0

// The setup procedure has not been finished yet.

4 Clocks and interfaces

4.1 Selection of Clock Sources

a) Select clock for PLL circuit

JP37 = 3-2 ➔ CK_TO_PLL= CLOCK40DES1
select TTC clock directly from TTCrx chip ***(default)***
JP37 = 1-2 ➔ CK_TO_PLL= CLK_OSC
select oscillator clock *(for tests only)*

b) Make CLOCK_TTC using original or improved TTCrx clock

JP36 = 1-2 ➔ CLOCK_TTC= CLOCK40DES1
select original TTCrx clock ***(default)***
JP36 = 3-2 ➔ CLOCK_TTC= CLK40PLL
select improved TTC clock from PLL circuit

c) Select CLK_EXT, the external clock for TIM chip:

JP35 = 3-2 ➔ CLK_EXT= CLOCK_TTC
select TTC clock ***(default)***
JP35 = 1-2 ➔ CLK_EXT= CLK_X
select ECL/NIM clock from the Front Panel LEMO

d) Select clock inside TIM chip:

JP10 = 3-2 ➔ SEL_TTCLK = '1' select TTC clock ***(default)***
JP10 = 1-2 ➔ SEL_TTCLK = '0' select oscillator clock CLK_LOCAL

e) Select source for CLK_BACK going to the back-plane

Insert only one of 4 jumpers!

JP3= ON	selects CLK_TIM, clock of TIM chip ***(default)***
JP4= ON	selects CK_OSCB, oscillator clock
JP5= ON	selects CKTTCB, clock from TTCrx or from PLL circuit
JP31= ON	selects CK_XB, external clock from LEMO connector

f) Select source for VME chip:

Insert only one of 3 jumpers!

JP32= ON	selects CK_OSCV, oscillator clock ***(default)***
JP33= ON	selects CKTTCV, clock from TTCrx or from PLL circuit
JP34= ON	selects CK_XV, external clock from LEMO connector

g) Select source for CLK_LEMO that feeds the front panel LEMO connectors CKO1..12

Insert only one of 4 jumpers!

JP30= ON	selects CK_XF, external clock from LEMO connector
JP8= ON	selects CKTTCP, clock from TTCrx or from PLL circuit
JP6= ON	selects CK_OSCP, oscillator clock
JP7= ON	selects CLK_TIM_P, clock of TIM chip ***(default)***

The DLL circuit inside the TIM chip eliminates any delay of the TTCrx clock signal. The other fast signals (L1A, BCRES,...) going to the backplane are adjusted to the clock signal of the TIM chip.
For the data taking run select TTC clock in the TIM chip and send the TIM clock to the backplane, in other words set all switches and jumpers to their default positions. The other jumper and switch positions are used for various tests.

4.2 Front Panel Inputs

Optical TTC fibre from a TTCex board to the TTCrx mezzanine board that delivers the common CMS clock and synchronization signals.
External Clock CLK_X …=default LHC-clock input for GT crate.

Actually AC-coupling allows to apply either ECL or NIM signals for tests.
Later it might be changed to DC coupled negative ECL levels.

External L1A_X **//Input circuit changed to NIM levels for tests**
used to run readout tests to find highest possible L1A rate. Burst tests.
External BCRES_X (Bunch Counter Reset)
//Input circuit changed to NIM levels for tests.
//Later it might be changed to DC coupled negative ECL levels to receive the ORBIT signal from the TTCmi , the LHC –machine interface.
- to run with different orbit lengths,
- to run synchronously with other Trigger electronics (local tests) etc..

4.2.1 TTCrx signals

The signals are generated by a TTCvi board, go to a TTCex board and are sent via an optical fibre to the TTCrx receiver chip that is mounted on a TTCrx Mezzanine board on the TIM module.

Clock:	Clock 40, Clock 40Des1, Clock 40Des2;
Channel A:	L1Accept *with programmable Delay in bx*
Channel B:	
Broadcast Data Interface:	Brcst[7:2], EvCntRes, BCntRes; BrcstStr1, BrcstStr2;
Data Interface:	Dout[7:0], SubAddr[7:0], DQ[3:0], DoutStr
Counter Interface:	BCnt[11:0], EvCntHStr, EvCntLStr, BCntStrb

Internal Registers:
BCcntr 12 bits, EvCntr 24 bit...reset by broadcast Reset

4.3 Front Panel Outputs

MONX : returns the external CLK_X (LEMO input on front panel).
MON : general monitoring LEMO output. The SW6 switch selects the signals sources:

5-1 RESET_PAN	// RESET delayed for the Front Panel; from TIM chip
5-2 L1A_PAN	// L1A delayed for the Front Panel; from TIM chip
5-3 CLK_OSCM	// oscillator
5-4 CKTTCMON	// CLOCK_TTC = original or improved TTC clock

BCRES_TTC // BCRES delayed for the Front Panel; from TIM chip
CKO_1...12 Clock outputs; 40 MHz, 50 Ohm ABT driver (TTL level).
Source selected by jumpers. See 4.1 above. *In the GT-crate the clock outputs are connected to the Fast Signal Conversion boards and the Tracker Emulators (APVE).*
CKO_13...24 An additional set of 12 CLK signals is available if the TIM board is used in the GT crate and implemented with a 9U frontpanel.

4.4 Front Panel Buttons and LEDs

SW3 INACTIVE // If pushed it sets the TIM board into the 'inactive' state.
SW4 RUNNING // If pushed it sets the TIM board into the 'running' state.

DIO7 GREEN: L1A	// as sent to the back-plane
DIO7 RED: NTTCRX_ERR	// shows error in TTCrx chip
DIO6 GREEN: RUNNING	
DIO6 RED: INACTIVE	
DIO5 GREEN: TTCREADY	// TTCrx chip is ok
DIO5 RED: VME access is active	

4.5 Control signals via back-plane

4.5.1 Clock, L1A, BCR, L1Reset distribution up to version V1002

The TIM chip receives the common CMS 40 MHz clock and from the TTCrx chip the L1A (Level 1 Accept) and the messages Bunch Counter Reset (BCR or BCRes) and L1Reset. It sends the 4 signals as differential point-to-point signals (LVDS) via the back-plane to each board in the crate. The signals for each slot can be disabled by software if boards are not plugged in.

The signals L1A, RESET(or RESYNC), EVCNT_RES are encoded according to the table below. The signal BCRES is not encoded and is sent with a different delay.

			TIM signals via backplane	Delays applied
x	0	0	NOP	----
x	0	1	**RESET/RESYNC**	L1A_DLY_H/L
x	1	0	**L1A**	L1A_DLY_H/L
x	1	1	**EVCNT_RES**	L1A_DLY_H/L
1	x	x	**BCRES**	RES_DLY_H/L

4.5.1.1 Version V1003 DESIGN CHANGE to be done (Oct.2003)

L1A could arrive concurrently with BCRES or concurrently with STOP/GO.
The BGO commands are never sent concurrently and can be coded.

Agreement 20. Oct 03 with J. Eroe:

Therefore the encoding shown in table below will be implemented to send 5 BGO commands via 3 signal lines to the DTTF/GT boards.

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L1A	BCRES	L1RES	Command
0	0	1	L1RES /RESET/RESYNC
0	1	0	BCRES
0	1	1	EVENT CNTR RESET
1	0	0	L1A
1	0	1	GO/STOP *
1	1	0	Concurrent L1A , BCR
1	1	1	ORBIT CNTR RESET

Table 1 Encoded L1A and BGO commands

- The GO/STOP command forces an inactive circuit into the RUN state and a data taking circuit into the STOP state. The L1RES signal forces the circuit always into the stop-state.
- If L1A and GO/STOP appear at same time then GO/STOP will be sent at the next clock tick.

Remarks:

The other BGO commands (Test_EN, Private_GAP, Private_Orbit, HardRes) are not used in DTTF. DTTF sends calibration events like any other events during data taking runs. The calibration events are flagged in the data records.
DTTF and GT ignore Private Gaps and Orbits and also ‘private’ BGO commands.
It is assumed that no ‘official’ BGO cmds are sent during Private Gaps and Orbits.
The TIM chip inhibits L1A during STOP periods. Therefore GO and STOP commands are not required by GT, DTTF boards anymore?

4.5.1.2 Remark for GT crate

In the GT crate on each card a PLL clock driver chip regenerates the clock signal and broadcasts it to all chips on the board with a maximum phase difference of less than 1 ns. The PLL circuits are synchronised 40ms after the start of the clock signal. A 40 MHz on board oscillator can be used instead of the TTC clock for stand-alone tests.

4.5.2 Signals between TIM and TCS board (GT crate)

4.5.2.1 8 TIM to TCS signals ('Fast Signals')

The TIM board sends 5 Fast Signals to the TCS board:

(ATTENTION The TIM to TCS signals will be changed!!
We will encode the status bits and send them to the FDL board, to be combined with the status bits from the other GT boards!)

TIM_ERR *composed by an OR of:*

BAD_LOCAL_BC: *Difference between local BC counter and the TTCrx BC-number.*

BAD_MAX_BC: *The BCR signal arrives not at local BC count=3564.*

DBERR: *double bit error from TTCrx chip.*

TIM_OUT_OF_SYNC *composed by an OR of:*

ROBUF_SYNCERR

In addition to the derandomizing Readout Buffer FIFO for extracted data another FIFO containing the corresponding bunch crossing numbers runs in parallel. If the 'EMPTY' flags of both FIFOs disagree then this error flag will be set.

ROBUF_OVF

If the derandomizing Readout Buffer is full the next write access sets this error flag.

L1A_TOO_OLD

A L1A arrives with a constant latency at the L1A queue and waits to extract the corresponding data from the Ring Buffer memory to move them into the derandomizing Readout Buffer (RO-Buffer). If the waiting time of a L1A exceeds the equivalent of 15/16 of the Ring Buffer size then a monitoring circuit sets the error flag L1A_TOO_OLD.

TOO_MANY_L1A

If more than 63 L1A are waiting in the L1A-queue then this error flag appears.

TIM_WARNING_OVFLO:

L1A_OLD_WARN

A L1A arrives with a constant latency at the L1A queue and waits to extract the corresponding data from the Ring Buffer memory to move them into the derandomizing Readout Buffer (RO-Buffer). If the waiting time of a L1A exceeds the equivalent of 75% of the Ring Buffer size then a monitoring circuit sets the warning flag L1A_OLD_WARN.

WARNING_ROBUF_OVF

If 75% of the derandomizing Readout Buffer are occupied then this warning flag will be set.

TIM_READY

The TTCrx chip has to send a TTC-ready flag and the initialization program has to set the command register bit TIM_SETUPDONE =1 to tell the Trigger Control system on the TCS board that the TIM board is ready to run. The TTC-ready flag can be emulated by software when running without the TTC link..

TIM_BUSY

TIM_BUSY = 1 (active) as long as the initialization program has not set the command register bit TIM_SETUPDONE =1.

Other signals to the TCS board:

L1_RESET

To be explained later.

TI_INHIBIT_PHYS_L1A

To be explained later.

TI_INHIBIT_ALL_L1A

To be explained later.

4.5.2.2 8 TCS to TIM signals

L1A_FROM_TCS *will be used to check if the same L1A arrives also via the TTC optical link. Other 7 signals are not defined yet!*

4.5.3 Signals between TIM and FDL board (GT crate)

4.5.3.1 8 TIM to FDL signals

Not defined yet!

We will encode the status bits and send them to the FDL board, to be combined with the status bits from the other GT boards!)

4.5.3.2 8 FDL to TIM signals

Not defined yet!

4.5.4 Signals between TIM and GTFE board (GT crate)

4.5.4.1 1 TIM to GTFE signal

Not defined yet!

4.5.4.2 1 GTFE to TIM signal

GTFE_READY

GTFE_READY =1 allows the Readout Processor in the TIM chip to send event records as long as there are any in the RO-Buffer.

5 Synchronization and monitoring

Achtung dieser Teil muss noch erneuert werden

5.1 BX-Synchronisation inside the GT-crate by BcntRes

The BCRes is sent to the GTF and all PSB boards and starts at the same time the bunch crossing counters of the synchronisation circuits. At the end of the LHC cycle the contents of all Bunch counters on all boards are stored and then checked by a monitoring program. BCRes is sent every LHC cycle and resynchronises without loosing bx-data.

5.1.1 Readout of data: **See description of PSB too.**

In case of a L1Accept the TTCrx sends the Event counter high and low part and the bunch crossing number. An offset is subtracted from the BX number and a Event/Monitor Identifier is added to the Event-number. Then all three words and the 3 strobe signals are stored consecutively in a short FIFO and afterwards they are broadcasted in the same order to the GTF and all PSB modules, but with a frequency of 10 or 20 MHz to avoid time problems on the back-plane. The BcntrStrobe signal starts a Readout processor (ROP) on every board, which collects data from all Dual Port Memories and moves them to the GTFE link. As the first word the ROP sends the event number with the identifier.

5.1.2 Fast Readout of Monitoring data:

The Global Monitoring circuit on the TIM board extracts data from the DPMs of all boards simulating a L1Accept and uses the links of the event readout to collect data on the GTFE board. The Readout processors on the GTF and the PSBs insert a* monitoring identifier *into the event number word, which is used to move the monitoring data to the Monitor memory on the GTFE board. In average 2 monitoring request can be sent between two L1Acc. On the GTFE board monitoring data go into a special memory, which is read separately.

5.2 Orbit Monitoring request and special trigger to read statistics data

There are several counters in the GT crate which should be read every nth bunch crossing: Dead time counters, rate counter etc.
The pretrigger+trigger sequence is generated on the TIM module and starts with a data taking run. A 1/n counter with programmable rate generates this trigger.

5.2.1 Orbit Monitoring request:

There are several counters in the GT crate which should be read every nth bunch crossing. This trigger is generated on the TIM module and starts with a data taking run (calibration, monitoring, private or physics run). The rate is programmable.
A 1/n counter generates this trigger. The NewRun resets and the BcRes signal increments the counter. Every n orbits a EN_ORBIT_RESET saves and then resets all counters in the GT-crate with the next BcRes signal. During the next LHC orbit send a Mon_Trig Request to read all data to the FED module.

5.2.2 XON/XOFF: See GT-Overview too!!!

If the CMS DAQ cannot accept new event anymore it sends a XOFF signal. New L1Acc from the TTC system are inhibited but data for all pending readout requests are collected and transferred to the GTFE modules, where they wait in the DPMs for transfer. The Trigger logic continues to work but new triggers to the TTC system are suppressed.
In case of a fatal DAQ breakdown all events in the readout chain are cancelled.
The number of incoming but suppressed L1Acc's is counted.
BETTER: The CMS-DAQ should give a STOP message to the TTC system. The TTC should send an XOFF message to start dead time counters everywhere. Then it should send an XON to prepare all readout systems for the following L1Acc requests.

NO: ONE Deadtime counter in GT ONLY !!!!!

TTCrx: Normally the content of the TTCrx Bunch counter is present on the BCnt[11:00].
When a L1A arrives the following sequence of data is put onto the BCnt[11:00] bus.
L1Acc sequence:

Control Register(1,0)	Cycle	Sequences
00	0	Event counter low on bunch counter bus
01	*0*	*Bunch counter on bunch counter bus*
10	***0***	***Event counter low on bunch counter bus***
	1	***Event counter high on bunch counter bus***
11	**0**	**Bunch counter on bunch counter bus**
	1	**Event counter low on bunch counter bus**
	2	**Event counter high on bunch counter bus**

6 Power circuits

6.1 Backplane power

The DTTF crate provides +5V, +3.3V and the GT crate in addition +2.5V and 1.8V.
In the DTTF crate the voltage and GND pins occupy column 'C' of the 2 mm connectors.
In the GT crate column 'C' of the upper A, B, C 2-mm connectors is reserved for GND pins.
Column 'C' of the lower A, B, C 2-mm connectors are still undefined. The voltages in the GT crate occupy pins of the 160-pin VME connector.
The TIM board receives +5V, +3.3V via VME connector pins. Two GND pins, a +5V and a +3.3V pin make contact first to bias the VME signals and to disable output signals to the backplane if the TIM board is plugged into a living crate. See also chapter about Hot Swap circuit.

6.2 Onboard power-supply

There will be a +1,5V power-supply for the VIRTEX-II chip with 3A output-current.
National LP3966, low-drop-out, adj. 1,5V/3A, TO-220 or TO-263.
Input voltage: 3.3V

Other possible components:
Linear regulators:
National LP3965, low-drop-out, adj. 1,5V/1,5A, TO-220 or TO-263
National LM1085, adj. 1,5V/1,5A, TO-220 or TO-263
National LM1086, adj. 1,5V/3A, TO-220 or TO-263
Switching regulators:
Maxim MAX1843, 1,5V/2,7A, QFN-28

7 VME chip

8 Timing chip

8.1 Definition of Left-Right Slots in the 6u prototype GT crate

This table has been copied from B. Neuherz and is probably not controlled by others.

TIM card	BACKPLANE 6U	SLOT NR
L1	GTL2	14
L2	GTL1	13
L3	PSB6	12
L4	PSB5	11
L5	PSB4	10
L6	PSB3	9
L7	GMU1	7
L8	PSB1	5
R1	FDL1	16
R2	FDL2	17
R3	GTFE	18
R4	GTL3	19
R5	PSB7	20
R6	PSB8	21
R7	GMU2	8
R8	PSB2	6

8.2 VME addresses

A31 .....A24	A23 …A20	A19	A18		*Address Modes*
BASE ADDRESS_GT	xxxx	x	x		*Extended Base address*
xxxx xxxx not available	BASE ADDRESS_DTTF				*Standard Base address*

	A17	A16	A15…12	A11...8	A7...4	A3...A1, x
TIM chip	**0**	**1**	**a a a a**	**a a a a**	**a a a a**	**a a a 0**
registers	**0**	**1**	**0x**	**0x**	**00 –5E**	
TTCrxdump	**0**	**1**	**0x**	**0x**	**80 – 9E**	
Free space	**0**	**1**	**0x**	**0x**	**A0 – FE**	

Free space	**0**	**1**	**0x**	**100 – 1FFE**
BC-Table 4k W16	**0**	**1**	**2000 – 3FFE**	
RING BUFFER 1k W16	**0**	**1**	**4000 – 47FE**	
free *nn k W16*	**0**	**1**	**4800 – FFFE**	
Free space	*2 0000 – 3 FFFE*			

8.2.1 TIM chip registers

WARNING: 11.11.02 A.T.:
All register addresses have been changed to apply delays for up to 16+16=32 bx for L1A and L1_RESET/RESYNC and for the BCRES signals.

8.2.1.1 Delay Registers for boards on left and right side

The signals L1A, RESET(or RESYNC), EVCNT_RES are encoded according to table below. The signal BCRES is not encoded and is sent with a different delay.

- L1A = 'Level 1 Accept' trigger signal to read an event.
- RESET = signal to resynchronize the boards (other names L1_RESET or RESYNC).
- EVCNT_RES = resets the event counters after a resynchronization procedure.

Signals on backplane			2 bits are encoded to send EVCNT_RES	Delays applied	Remarks
BCres	L1a	Reset			
x	0	0	NOP	----	
x	0	1	**RESET/RESYNC**	L1A_DLY_H/L	*Use same delay value for 3 signals*
x	1	0	**L1A**	L1A_DLY_H/L	
x	1	1	**EVCNT_RES**	L1A_DLY_H/L	
1	x	x	**BCRES**	RES_DLY_H/L	

The total delay consists of (DLY_L +1) + (DLY_H +1). Each hex-number programs a 15bx delay circuit. The value 'F' means 'no delay'. The minimum delay 'FF' =0 bx and the maximum delay 'EE'=30 bx.
DLY_L1 is the delay for the next board on the left side of the TIM6U module, DLY_L2 for the 2nd on the left side and so on. DLY_R1…R8 define the delays for boards on the right side.

Address A17-A0	Registername	D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
1 0000	DLY_L1	L1A_DLY_H				L1A_DLY_L				RES_DLY_H				RES_DLY_L			
1 0002	DLY_R1	L1A_DLY_H				L1A_DLY_L				RES_DLY_H				RES_DLY_L			
1 0004	DLY_L2	L1A_DLY_H				L1A_DLY_L				RES_DLY_H				RES_DLY_L			
1 0006	DLY_R2	L1A_DLY_H				L1A_DLY_L				RES_DLY_H				RES_DLY_L			
1 0008	DLY_L3	L1A_DLY_H				L1A_DLY_L				RES_DLY_H				RES_DLY_L			
1 000A	DLY_R3	L1A_DLY_H				L1A_DLY_L				RES_DLY_H				RES_DLY_L			
1 000C	DLY_L4	L1A_DLY_H				L1A_DLY_L				RES_DLY_H				RES_DLY_L			
1 000E	DLY_R4	L1A_DLY_H				L1A_DLY_L				RES_DLY_H				RES_DLY_L			
1 0010	DLY_L5	L1A_DLY_H				L1A_DLY_L				RES_DLY_H				RES_DLY_L			
1 0012	DLY_R5	L1A_DLY_H				L1A_DLY_L				RES_DLY_H				RES_DLY_L			
1 0014	DLY_L6	L1A_DLY_H				L1A_DLY_L				RES_DLY_H				RES_DLY_L			
1 0016	DLY_R6	L1A_DLY_H				L1A_DLY_L				RES_DLY_H				RES_DLY_L			

1 0018	DLY_L7	L1A_DLY_H	L1A_DLY_L	RES_DLY_H	RES_DLY_L
1 001A	DLY_R7	L1A_DLY_H	L1A_DLY_L	RES_DLY_H	RES_DLY_L
1 001C	DLY_L8	L1A_DLY_H	L1A_DLY_L	RES_DLY_H	RES_DLY_L
1 001E	DLY_R8	L1A_DLY_H	L1A_DLY_L	RES_DLY_H	RES_DLY_L
1 0020	DLY_L9	L1A_DLY_H	L1A_DLY_L	RES_DLY_H	RES_DLY_L
1 0024	DLY_TIM*	L1A_DLY_H	L1A_DLY_L	RES_DLY_H	RES_DLY_L
1 0026	DLY_PAN+	L1A_DLY_H	L1A_DLY_L	RES_DLY_H	RES_DLY_L

**) GT-only: DLY_TIM defines the delays for the Readout logic in the TIM chip.*
+) DLY_PAN defines delays for the front panel signals RESET_PAN, BCRES_PAN and L1A_PAN.

8.2.1.2 DISABLE Boards in Crate

Address A17-A1	Registername	D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
1 0022	DIS_ BOARDS	L 8	R 8	L 7	R 7	L 6	R 6	L 5	R 5	L 4	R 4	L 3	R 3	L 2	R 2	L 1	R 1
	default values	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*0*

EXAMPLE: BIT D14=1 disables board L(eft) 7
DIS_BOARD_L9: *See COMMAND register bit11 in 8.2.1.10.*

8.2.1.3 CRATE delays

If the ORBIT ECL signal is used as the bunch counter reset signal BCRES then the DLY_CRATE_ECL is used to adjust the DTTF respectively the GT crate to the LHC orbit.
If BCRES from the TTCrx chip is used then the adjustment is done either by programming the TTCrx chip or by programming the DLY_CRATE_TTC register.
Total delay = 1 + delay[15:0].
Warning: The circuit uses a 16-bit counter and therefore the delay value has to be set smaller then 3564. Otherwise the previous BCRES will be suppressed.

Address A17-A1	Registername	D15 ……D0
1 0028	DLY_CRATE_TTC	*value < 3564; default =0*
1 002A	DLY_CRATE_ECL	*value < 3564*

8.2.1.4 UNUSED Registers

The registers are free. Old version contained CHIP_ID H/L, that is now at 1 0060.

Address A17-A1	Registername	D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
1 002C	xxxxxxxxx	*free*															
1 002E	xxxxxxxxx	*free*															

8.2.1.5 SIMULATION PERIODS

The registers define the time (unit=1 LHC orbit) between active orbits. During an active orbit simulated Trigger signals or BGO commands or UserMessages are sent according to the values in the BC-Table. If xx_PERIOD=0 then the messages are sent every orbit. See also chapter PERIODIC SIMULATION

Address A17-A1	Registername	D15 ……. D0

1 0030	TRIG_PERIOD	*Period for L1A and MonRqst signals*
1 0032	BGO_PERIOD	*Period for Bgo signals and UserMessages*

8.2.1.6 OBIT LENGTH

Address A17-A1	Registername	D15-D12	D11 – D8	D7 – D4	D3 – D0
1 0034	ORBIT_ LENGTH	16 bit number			
	Default value	***0***	***D***	***E***	***A***

The ORBIT_LENGTH defines the length of the LHC orbit. Default value =3564-2 (= 0DEA hex) bunch crossings. *The BC counters run from 0 until 3564 – 1=3563. For simulation the value 200 -2='00C6\H' has been used.*
The orbit length is used to reset the bunch crossing counter if the BCRES signal is missing, for example when running without LHC signals in LHC orbit simulation mode.
The logic consists of a 16-bit counter+16 bit comparator. The upper 4 bits are always zero.
Check1: The programmed BC LIMIT is compared against the content of the local BC-counter at the arrival time of the common BCRES signal. Any difference sets the error flag BAD_MAX_BC. *The reason for this error could be a bad clock signal or a bad BCRES signal.*
Check2: The local BC-counter is compared against the BC-number from the TTCrx chip. The difference can be read by VME. A change in the difference sets the error status bit BAD_LOCAL_BC.
Remark: For Heavy Ion runs every 5th tick contains a bunch crossing.

8.2.1.7 TTC_Message_Subaddress register

Address A17-A1	Registername	D15-D12	D11 – D8	D7 – D4	D3 – D0
1 0036	TTC SUBADDRESS	Last TTC Message *(read only)*		TTC Subaddress *(write/read)*	

- TTC Subaddress defines the address for individual addressed messages/commands. The command byte is stored in the last address ("…F") of the TTC_DUMP memory. See also chapter 8.2.2. Functions for individual messages are neither defined nor implemented.
- Last TTC Message contains the last system and user message code that has been received from the TTCrx chip.

8.2.1.8 COMMAND PULSE

Set the COMMAND REGISTER bits before sending COMMAND PULSES (bit11…0)
Warning: The VME instruction generates a pulse when a data bit is set equal 1. This "register" cannot be read back ('write only').
The command bits 0…9 are used to simulate the corresponding BGo commands, which are received during data taking by the TTCrx link. See also CMD register 8.2.1.10. **The command pulses (bits 11 to 0) can be used only if the SELECT bits in the Command Register have been set before.**
HARD_RES_VME will stop in any case the BC-Table signal generation.

Address A17-A1	Registername	D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
1 0038	COMMAND PULSE	*See description of bits below.*															
	default values	-	-	-	-	-	-	-	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*0*

Bit 15: **RESET_TTCRX**
RESET_TTCRX =1 sets the RESET_TTCRX Flip-Flop=1 to put the TTCrx into the 'RESET' status. *RESET_TTCRX must not be done during a data-taking run!!!*

Bit 14: **RELEASE_TTCRX**
After several microseconds send RELEASE_TTCRX =1 that clears the RESET_TTCRX Flip-Flop to remove the 'RESET' status of TTCrx chip.

Bit 13: **MONRQST_VME**
MONRQST_VME =1 sends a Monitoring Request.

Bit 12: **SEND_TESTDATA**
SEND_TESTDATA =1 sends test data to all ROPs

Bit 11: **L1A_VME**
L1A _VME=1 simulates a L1A signal, *if SEL_L1A_[2:0]=000 has been set before.*

Bit 10: *not used*

Bit 9: **DO_TEST_EN_VME+)**
DO_TEST_EN_VME =1 sends the command to all GT board to run a calibration cycle, *if SEL_BGO_1,0 =00 has been set before.*

Bit 8: **DO_PRIV_GAP_VME+)**
DO_PRIV_GAP_VME =1 sends the command to all GT board to run a private gap procedure, *if SEL_BGO_1,0 =00 has been set before.*

Bit 7: **DO_PRIV_ORBIT_VME+)**
DO_PRIV_ORBIT_VME =1 sends the command to all GT board to run a private orbit procedure, *if SEL_BGO_1,0 =00 has been set before.*

Bit 6: **RES_ORBIT_VME+)**
RES_ORBIT_VME =1 sends a RESET ORBIT counter command, *if SEL_BGO_1,0 =00 has been set before.*

Bit 5: **START_RUN_VME+)**
START_RUN_VME =1 sets RUN_FF to allow L1A signals to be sent to the boards, *if SEL_BGO_1,0 =00 has been set before.*
The RUN_FF can also be changed by a periodic BGo command, by a BGo from TCS or by a TTC message.

Bit 4: **STOP_RUN_VME+)**
STOP_RUN_VME =1 clears RUN_FF to inhibit L1A signals, *if SEL_BGO_1,0 =00 has been set before.*

Bit 3: **EVCNT_RES_VME *)**
Resets the Event Counter by VME, *if SEL_* EVRES*_1,0 =00 has been set before.*

Bit 2: **L1RES_VME *)**
Send a L1RESET to all boards (alias names RESET, RESYNC), *if SEL_BGO_1,0 =00 has been set before.*
See also chapter 8.3.2 below.

Bit 1: **HARD_RES_VME+)**
Used inside TIM chip only, *if SEL_BGO_1,0 =00 has been set before.*
See also chapter 8.3.1 below.

Bit 0: **BCRES_VME*)**
BCRES_VME =1 sends a bunch counter reset signal, *if SEL_BCRES_[2:0] =000 has been set before.*
For internal orbit generation send BCRES_VME once to start the BC counter logic if there is no TTC connected. Afterwards LHC orbits will be simulated according to the ORBIT_LENGTH register.

**) This command is also sent sent as a fast LVDS signal via the back-plane to all boards in the DTTF and GT crate.*
+) This 'slow command' is sent via the back-plane ROP bus to all boards in the GT crate; but not in the DTTF crate.

8.2.1.9 STATUS Register

Warning:
The read-only STATUS register has got the same VME address as the CMD-Pulses.

Address A17-A1	Registername	D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
1 0038	STATUS Register	*See description of bits below.*															

Bit15 – 6 show the status of the TIM Readout circuits and used in the GT crate only.

Bit 15: **OV_BAD_TTC**
OV_BAD_TTC =1: Overflow bit of BAD_L1A_TTC counter counting the number of not concurrent L1A from TCS and TTC.

Bit 14: **TOO_MANY_L1A**
TOO_MANY_L1A = 1: More than 64 L1A are waiting in the request queue whose data have to be extracted from the RingBuffer. *(GT crate only.)*

Bit 13: **L1A_TOO_OLD**
L1A_TOO_OLD = 1: The L1A are waiting in the request queue for more than 960 bunch crossings corresponding to 15/16 of the RingBuffer size. The write pointer is only 64 bunch crossings behind the read pointer and will overtake it soon overwriting the events of the pending L1A's. *(GT crate only.)*

Bit 12: **L1A_OLD_WARNING**
L1A_OLD_WARNING = 1: The L1A are waiting in the request queue for more than 768 bunch crossing corresponding to ¾ of the RingBuffer size. The distance between the write- and the read pointer has decreased already to ¼ of the Ringbuffer. *(GT crate only.)*

Bit 11: **ROBUF_OVF** *// overflow of derandomizing readout buffer*
ROBUF_OVF = 1: The readout buffer FIFO containing the event data is full. More than 'nn' events are already waiting to be transferred to the GTFE board.
'nn' = 1024/3 =341 for readout of 3 bx per L1A.

Bit 10: **WARNING_ROBUF_OVF**
WARNING_ROBUF_OVF = 1: The readout buffer FIFO is filled up to the warning level of 75%. *The TCS (Trigger Control) should decrease the trigger rate.*

Bit 9: **ROBUF_SYNCERR**
ROBUF_SYNCERR = 1: The readout processor ROP didn't read the event data correctly because the FIFO's for trigger data and the bx-number became empty at different time.

Bit 8: **EVNR_OVF**
EVNR_OVF = 1: There was an overflow of the 24 bit Event counter. The bit is used just for information. *It is not an error bit!*

Bit 7: **BAD_LOCAL_EV**
The local and the TTCrx event number are compared to each other. In case of any difference the error bit BAD_LOCAL_EV is set to 1.

Bit 6: ***not used***

Bit 5: ***not used***

Bit 4: **BAD_MAX_BC**

BAD_MAX_BC=1: The local bunch crossing counter does not agree with the ORBIT_LENGTH at arrival time of the BCRES signal.

Bit 3: **BAD_LOCAL_BC**

The local and the TTCrx bunch crossing numbers are compared to each other. If the difference changes then the error bit BAD_LOCAL_BC is set to 1.

Bit 2: **SINERR_TTCRX**

SINERR_TTCRX=1: There was a single bit error in the TTCrx chip.

Bit 1: **DBERR_TTCRX**

DBERR_TTCRX=1: There was a double bit error in the TTCrx chip. It was not corrected.

Bit 0: **TTC_READY**

TTC_READY=1: The TTCrx chip is working correctly.

8.2.1.10 COMMAND Register

Set the COMMAND REGISTER bits before sending COMMAND PULSES.

Address A17-A1	Registername	D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
1 003A	COMMAND Register							SEL_ EV RES		SEL_ BGO		SEL_ BCRES			SEL_ L1A		
	default values	*1*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*1*

Bit 15: **TIM_SETUPDONE**

TIM_SETUPDONE =1 to tell the TCS board that the setup of the TIM board is done. *This bit sets the Fast Signals TIM_READY and clears TIM_BUSY that can be checked on the TCS board. This bit should be set at the end of a TIM-board-Setup-Program. See also 3.8 Fast Signals to TCS board.*

Bit 13: **TTC_RDY_VME**

The bit is used to simulate a TTC_RDY status´.

Bit 12: **CHECK_TTC_CHAIN**

CHECK_TTC_CHAIN =1 checks if every L1A received directly from the TCS board has also been received via the optical TTC fiber. *The L1A_TCS_DLY delays the L1A sent by the TCS board over the backplane so that it arrives concurrently with the L1A sent via the TTC fiber. See also L1A_TCS_DLY register in 8.2.1.12 below.*

Bit 11: **DIS_BOARD_L9**

DIS_BOARD_L9 =1 stops timing signals to the L9 board. See also 8.2.1.2 for other boards.

Bit 10: **DIS_RO_BUS**

DIS_RO_BUS =1 disables the Readout Request bus (GT crate only).

SELECT 'EVENT COUNTER RESET'

Bit9: SEL_EVRES_1,

Bit8: SEL_EVRES_0

Code Bits 9-8	Selected source of EVENT COUNTER RESET command
00	Only the VME generated EVENT COUNTER RESET is allowed.
01	Take EVCNTRES signal of the TTCrx chip //=default in DTTF and GT crates
10	Take EVENT COUNTER RESET from the active/selected BGO source

11	*Inhibit any EVENT COUNTER RESET*

SELECT source of BGO commands
Bit7: SEL_BGO_1,
Bit6: SEL_BGO_0

Code Bits 7-6	Selected source of BGO commands
00	Only VME generated BGO commands are allowed.
01	BGO from TTCrx chip //=default in DTTF and GT crates
10	Periodic BGO internally generated
11	BGO from TCS board via back-plane

The same selection is valid also for the 'USER MESSAGES', which are generated either periodically or by the TTC system.

SELECT BCRES
Bit5: SEL_BCRES_2
Bit4: SEL_BCRES_1
Bit3: SEL_BCRES_0

Code Bits 5-3	Selected source of BCRES signal
000	Only VME command 'BCRES_VME' is allowed.
001	BCNTRES from TTCrx chip // = default in DTTF crates
010	ORBIT_X from Front Panel (ECL/NIM signal) // =default in GT crate
011	Periodic BCRES internally generated by BC-counter and comparator.
100	BGO command decoder. See also selected source of BGO commands
others	*Codes 101..111 inhibit all sources of BCRES*

Select the BCNTRES signal from the TTCrx chip only if it is sent every orbit.
Use the internally generated BCRES if the TTC system does not send a BCNTRES every orbit. In that case also the ORBIT_LENGTH has to be loaded with the correct value.
The periodic BCRES generator is started either by infrequent BCNTRES of the TTC system or by a VME instruction.
The Global Trigger will take the ECL CLK and ORBIT_X signals to run as precise as possible.

SELECT L1A
Bit5: SEL_L1A_2
Bit4: SEL_L1A_1
Bit3: SEL_L1A_0

Code Bits 2-0	Selected source of L1A signal
000	Only VME command 'L1A_VME' is allowed.
001	L1ACCEPT from TTCrx chip //=default in DTTF and GT crates
010	L1A_X from Front Panel (ECL/NIM signal)
011	Periodic L1A internally generated using the BC-Table
100	L1A from TCS board via back-plane
others	*Codes 101..111 inhibit all sources of L1A*

8.2.1.11 Readout_Command Register

This register is used in GT crate only.

The register contains the control bits to extract data on the TIM chip in case of a L1A.
This logic might not be used.

Address A17-A1	Registername	D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
1 003C	ROCMD _REG	*See description of bits below.*															
	default values	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*0*

Bit15-12: Write and read accesses are possible but the bits are not used by the control logic.

Bit 11: **RO_LINK_ON**

RO_LINK_ON=1 enables the Channel Link chip to allow transmission of event data to the GTFE readout board.
Default = 0 because normally TIM data are not included into the event data.

Bit10-9: Write and read accesses are possible but the bits are not used by the control logic.

Bit 8: **EN_BC_CHECK =1**

- Checks BC number at arrival time (=3564) of BCRES
  - ➔ *Status bits: ERR_MAX_BC, BAD_MAX_BC*
- Compare local BC counter with TTC BCnr
  - ➔ *Status bits: ERR_LOCAL_BC, BAD_ LOCAL_BC*

Bit 7: **EN_TTC_CHECK=1**

Checks if L1A from TTC and L1A from TCS arrive concurrently.
- ➔ *Status bits: ERR_L1A_TTC, BAD_ L1A_TTC*

Bit 6: **EN_EVNR_CHECK=1**

Compares with TTC EVnr with local Evcntr
- ➔ *Status bits: ERR_LOCAL_EV, BAD_ LOCAL_EV*

Bit 5: **EN_L1AQUEUE_CHECK=1**

The L1AQUEUE will be checked all the time. The check logic generates the warning bit L1A_OLD_WARN and the sync-error bits L1A_TOO_OLD and TOO_MANY_L1A. See bit 1 below how to stop the L1AQUEUE completely.
EN_L1AQUEUE_CHECK=1 allows to send the warning and sync-error states as Fast Signals to the TCS board.

Bit 4: **EN_ROBUF_CHECK**

EN_ROBUF_CHECK=1 checks if the readout buffer ROBUF is almost or really full. In these cases the warning bit WARNING_ROBUF_OVF and the sync-error bit ROBUF_OVF are set and sent also to the TCS board.

Bit 3: **FREEZE_RIBUF_IF_ERROR**

FREEZE_RIBUF_IF_ERROR =1 inhibits data transfer into the RING BUFFER in case of an error. This bit is useful to check the monitored data after an error.

Bit 2: **FREEZE_RIBUF**

FREEZE_RIBUF =1 inhibits data transfer into the RING BUFFER. This bit is used for tests with constant RING BUFFER content.

Bit 1: **INHIB_L1A_ON_TIM**

INHIB_L1A_ON_TIM =1 inhibits L1A's on the TIM board to remove TIM data from the Event data

Bit 0: **INVERT_ROPMUX**

INVERT_ROPMUX =1 inverts the clock for the ROP multiplexer. The multiplexer combines the 40 MHz L1A-event and monitoring data into phase A and phase B of 80 MHz parallel data to be transmitted by a Channel Link to the GTFE readout board. See page 9 of TIM chip schematic. The bit defines time order.
Default: INVERT_ROPMUX =0 sends the L1A-event first in phase A.
(to be checked???)

8.2.1.12 Delay L1A from TCS Register

The L1A_TCS_DLY delays the L1A sent by the TCS board over the backplane so that it arrives concurrently with the L1A sent via the TTC fiber. See also bit 12 in the CMD register 8.2.1.10 above.

The total delay consists of (DLY_L +1) + (DLY_H +1). Each hex-number programs a 16bx delay circuit. ***The value 'F' means 'no delay'***. The minimum delay 'FF' =0 bx and the maximum delay 'EE'=32 bx.

Address A17-A1	Registername	D15 .....D8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
1 003E	DLY_L1A_TCS	Not used	RES_DLY_H				RES_DLY_L			

8.2.1.13 ROBUF_PAR Register

Address A17-A1	Registername	D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
1 0040	ROBUF_ PAR	*NR_ROBUF*								*RO_LENGTH*							

Used by GT only.
Write and read access.
RO_LENGTH = < 255 (1024 / #of BC per event)
Examples: max=1024/3 =341; max=1024/5=204)

8.2.1.14 Record Identifier Register

Address A17-A1	Registername	D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
1 0042	IDENTIFIER	*Record Identifier for readout data*															

Used by GT only.
Write and read access.

8.2.1.15 IDLE_VALUE Register

Address A17-A1	Registername	D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
1 0044	IDLE_ VALUE	*Code for IDLE word between readout records*															

Used by GT only.
Write and read access.

8.2.1.16 EOF_VALUE Register

Address A17-A1	Registername	D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
1 0046	EOF_ VALUE	*Code for EOF (=end of file) word in readout record*															

Used by GT only.
Write and read access.

8.2.1.17 TESTDATA Register

Address A17-A1	Registername	D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
1 0048	TESTDATA	*Test data for RO_RQST bus*															

Used by GT only.
Test data to be sent via the RO-RQST bus to the boards in the crate.
Write and read access.

8.2.1.18 MON_RQST ID Register

Address A17-A1	Registername	D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
1 004A	MON_RQST _ID	*Identifier for Monitoring RQST*															

Used by GT only.
Identifier is used to distinguish Monitoring data from L1A data in the GTFE board.
Write and read access.

8.2.1.19 ROBUF_BX FIFO Register

Address A17-A1	Registername	D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
1 004C	ROBUF_BX FIFO	**BC number corresponding to trigger data in ROBUF_A FIFO**															

Used by GT only.
NO Write Access!! Read access only.

8.2.1.20 ROBUF_A FIFO Register

Address A17-A1	Registername	D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
1 004E	ROBUF_A FIFO	**Data bits of BC as stored in ROBUF_BX FIFO**															

Definition of data bits has to be done.
Used by GT only.
NO Write Access!! Read access only.

8.2.1.21 NBAD_L1A_TTC Register

Address A17-A1	Registername	D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
1 0050	BAD_L1A_ TTC Register	*See description of bits below.*															

Read access only.

8.2.1.22 BCDIFF Register

Address A17-A1	Registername	D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
1 0052	BC_DIFF Register	*BC difference between local BC counter and TTCrx*															

Read access only. To check for hardware errors.

8.2.1.23 MAX_BCNR Register

Address A17-A1	Registername	D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
1 0054	MAX_ BCNR Register	*Maximum value of Bunch Crossing Counter*															

Read access only. To check for hardware errors.

8.2.1.24 TTC_BCNR Register

Address A17-A1	Registername	D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
1 0056	TTC_BCNR Register	*Bunch counter number from TTCrx chip.*															

Read access only.

8.2.1.25 LOC_EVNR_H Register

Address A17-A1	Registername	D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
1 0058	LOC_EVNR _H Register	*High part of Local Event number*															

Read access only.

8.2.1.26 LOC_EVNR_L Register

Address A17-A1	Registername	D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
1 005A	LOC_EVNR _L Register	*Low part of Local Event number*															

Read access only.

8.2.1.27 TTC_EVNRH Register

Address A17-A1	Registername	D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
1 005C	TTC_EVNR H	*High part of Event number from the TTCrx chip*															

Read access only.

8.2.1.28 TTC_EVNRL Register

Address A17-A1	Registername	D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
1 005E	TTC_EVNR L	*Low part of Event number from the TTCrx chip*															

Read access only.

8.2.1.29 CHIP IDENTIFIER Registers

The DAQ group wants 32 bit identifiers for the chips. This address is reserved for that purpose. The bit format is preliminary.

Address A17-A1	Registername	D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
1 0060	CHIP_ID_H	*chip type bits 31...16: =0001 for GT crate*															
1 0062	CHIP_ID_L	*chip type bits 15…0: =42x1 /hardwired by design*															

Bits 15-12: = 4 for TIM card Bits 12 - 8: = 2 for TIM chip
Bits 7 - 4: = card# Bits 3 - 0: = 1 chip# *//There is only 1 TIM chip on board.*

8.2.1.30 CHIP VERSION Registers

Version numbers 1…1000(hex) are test designs.
Version numbers 1000…FFFF FFFF (hex) are standard designs.

Address A17-A1	Registername	D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
1 0064	CHIP_ VERSION_H	*Version number bits 31…16*															
1 0066	CHIP_ VERSION_L	*Version number bits 15…0*															

Example: Version_1001: CHIP_VERSION_H = 0000; CHIP_VERSION_L = 1001

8.2.2 TTC dump addresses

The 16 addresses below contain the TTCrx registers of the last dump action. See also description of TTCvi module and of TTCrx chip.
Only lower 8 bits are used. Read access only.

Address A17-A1	Registername	D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
1 0080	xxxx	----------								*xxxx*							
1 0082	xxxx	----------								*xxxx*							
1 0084	xxxx	----------								*xxxx*							
1 0086	xxxx	----------								*xxxx*							
1 0088	xxxx	----------								*xxxx*							
1 008A	xxxx	----------								*xxxx*							
1 008C	xxxx	----------								*xxxx*							
1 008E	xxxx	----------								*xxxx*							
1 0090	xxxx	----------								*xxxx*							
1 0092	xxxx	----------								*xxxx*							
1 0094	xxxx	----------								*xxxx*							
1 0096	xxxx	----------								*xxxx*							
1 0098	xxxx	----------								*xxxx*							
1 009A	xxxx	----------								*xxxx*							
1 009C	xxxx	----------								*xxxx*							
1 009E	xxxx	----------								*xxxx*							

8.2.3 BC – Table for Simulation

Address range: 0 2000 – 0 3FFE for 4k memory of BC table
The address corresponds to the bunch-crossing (BC) number. During Signal generation a BC-counter provides the read addresses. If a bit in the BC-Table is set to '1' at address 'aa' then a signal pulse will be sent at BC-number 'aa'. The signals are sent every n-th orbit as defined by the SIMULATION PERIOD register.
Bit 15-12 not implemented; VME access is not possible
Bit11,10: function not defined; VME access is possible
Bit 9: PER_MONRQST // sends a trigger to read out monitoring data.
Bit 8: PER_L1A // sends a trigger to read event data; periodic simulation of L1A
Bit 7: MESSG_SIM7 // simulate message bit 7 for user messages
Bit 6: MESSG_SIM6 // simulate message bit 6 for user messages
Bit 5: SIM_USR_MESSG_STRB // simulate user message strobe
Bit 4: PER_BGO_4 // simulate a BGO STROBE command

Bit 3: PER_BGO_3 // simulate bit3 of a BGO command
Bit 2: PER_BGO_2 // simulate bit2 of a BGO command
Bit 1: PER_BGO_1 // simulate bit1 of a BGO command
Bit 0: PER_BGO_0 // simulate bit0 of a BGO command

8.2.3.1 BGO codes

0000 = *not used*
0001 = *'BC0'…not used in TIM chip*
0010 = TEST_ENABLE
0011 = PRIVATE_GAP
0100 = PRIVATE_ORBIT
0101 = L1RESET (or RESYNC)
0110 = HARD_RESET
0111 = RESET_EVENT_COUNTER
1000 = RESET_ORBIT
1001 = START RUN
1010 = STOP RUN
1011…1111….*free for private purpose*

8.2.4 RING BUFFER 1k memory

Address range: 0 4000 – 0 47FE for 1k memory of Ring buffer.
First set FREEZE_RIBUF=1 to stop any input data and set INHIB_L1A_ON_TIM=1 in the RO_CMD register to stop triggered readout. Then it is possible to access the Ring Buffer memory by VME.
To check external or simulated signals often just freeze the Ring Buffer and read data from all addresses.
INPUT bits for the Ring-buffer:

Bit15: L1A_FROM_TCS *// arrives via the back-plane from the TCS board*
Bit 14: L1A_FROM_TCS_DLYED *// check programmed delay*
Bit13: L1A_FROM_TTC *// Bit 13 and 14 should appear at the same time*
// if the delay for L1A_TCS is set correctly.
Bit12: L1A_FROM_LEMO *// External trigger input*
Bit11: PER_MONRQST *// simulated periodic Monitoring Request*
Bit10: PER_L1A *// simulated periodic L1A*
Bit 9: 0 *// not used*
Bit 8: RES_EVCNT *// RESET Event Counter generated by any source*
Bit 7: ORBIT_P *// Pulse at begin of ORBIT signal (LEMO, ECL)*
Bit 6: BCRES_LEMO *// Delayed BCRES from Orbit signal*
Bit 5: BCNT_RES_TTC *// Bunch Counter Reset from TTC*
Bit 4: BCRES_TTC *// Bunch Counter Reset from TTC after optional delay*
// BCRES_LEMO and BCRES_TTC should appear at the same time if both are connected.
Bit 3: L1_RESET *// generated by any source*
Bit 2: PRIV_ORBIT *// generated by System Message or any BGO command*
Bit 1: PRIV_GAP *// generated by System Message or any BGO command*
Bit 0: TEST_EN *// generated by System Message or any BGO command*

8.3 RESET trees

The L1_RESET signal is forwarded to all boards in the VME crate. HARD_RES is used only inside the TIM chip. Both reset signals are generated either by software (VME) or by BGo signals arriving from the TCS (Trigger Control System) via the TTC optical link or by Message signals from the TTC link or are simulated periodically by the BC Table

8.3.1 HARD_RES

Signal sources:

- HARD_RES_VME *(software)*
- HARDRES_MSG: r*eceived as MESSAGE bits from TTC*
- HARDRES_BGO:
  - TCS_BGO: BGO signals received from TCS via TTC links
  - PER_BGO: BGO signals simulated by the BC-TABLE inside the TIM chip

Functions:

- HARD_RES_VME resets EN_BCTABLE circuit.
- HARD_RES = HARD_RES_VME + HARDRES_MSG + HARDRES_BGO
  - Clears the local EVENT COUNTER
  - Is combined with L1_RESET to make CLR_ALL (see below).

8.3.2 L1_RESET

Signal sources:

- L1RES_VME *(software)*
- L1RES_MSG: *received as MESSAGE bits from TTC*
- L1RES_BGO:
  - TCS_BGO: BGO signals received from TCS via TTC links
  - PER_BGO: BGO signals simulated by the BC-TABLE inside the TIM chip

Functions:

- L1_RESET resets/resynchronizes all boards in the VME crate.
- **Inside the TIM chip???**
- Is combined with HARD_RES to make CLR_ALL (see below).

8.3.3 CLR_ALL

- Resets error flag and checking counters
- Resets the RUN_FF, TEST_ENABLE
- Resets the L1A_queue and the ROP_EVENT controller circuit (for GT crate only)

8.3.4 STOP_RUN

- STOP_RUN also clears TEST_ENABLE FF

8.4 Pin assignment TIM chip

The TIMING chip is a FPGA from XILINX, called XC2V1000-4FG456C. There is an EXCEL-file containing the pin assignment of the TIM CHIP (see tim_chip.xls). The pintable is extracted from the XILINX datasheet of the FG456-package (ds031-4.pdf). (Extraction was done using Acrobat Reader 4.0 with ***Zusatzmodule/ACE*** enabled or using Acrobat4. Select the table that should be extracted and use right-mouse-button ***Extract Table.*** Save it as text file. Start EXCEL , open the text file and convert it. Do the same for each page.
The batch-file *..\tim_check\make_pin_nr_tim_chip.bat* provides a possibility "**to make" pin-numbers** of symbols in VIEWDRAW from the EXCEL-file.
The batch-file *..\tim_check\check_symbol_tim_chip.bat* provides a possibility "**to compare" pin-numbers** of symbols and the EXCEL-file (text-file of EXCEL-sheet). The comparision output is written into the file *..\tim_check\tim_check_symbol.log*

8.5 Symbol names

The naming convention of the symbols for VIEWDRAW schematics of Timing chip (..\Tim6U\sym):

tim.1	→	Timing chip
tim_clk.1	→	CLocK generation for distribution in GTL crate
tim_conf.1	→	XILINX CONFiguration pins of Timing chip
tim_jtag.1	→	JTAG pins of Timing chip

tim_pan.1 → signals from/to front-I/O (PANel)
tim_rop.1 → ReadOutProcessor unit in Timing chip
tim_rorq.1 → ReadOutReQuest unit in Timing chip
tim_term.1 → TERMination-resistors feature in Timing chip
tim_tsig.1 → fast Timing SIGnals
tim_ttc.1 → signals from/to TTCrx chip
tim_ttfg.1 → signals from Timing chip to TCS, FDL card and GTFE card
tim_vme.1 → signals from/to VME chip

8.6 Configuration ??

PROM CHIP….Preis, Lieferzeiten ???

Text fehlt noch!!!!

Configuration methods
Configure by VMEbus
Configure by PROM
Configure by JTAG

8.7 Special functions

8.7.1 Power-On Power Supply Requirements

The V CCINT , V CCAUX , and V CCO power supplies shall ramp on no faster than 100 ms and no slower than 50 ms. V CCAUX and V CCO for bank 4 must be connected together. If any V CCO bank powers up before V CCAUX , then each bank draws up to 600 mA (=transient current peak; does not harm the device)

Power On current	XC2V1000
I_{CCINT_MIN}	500 mA
I_{CCAUX_MIN}	250 mA
I_{CCO_MIN}	10 mA

8.7.2 Power-down sequence

The command register bit PWRDWN=1 in the VME chip assigns the PWRDWN_B signal (active low) to set the TIM chip into a low-power, inactive mode. The bi-directional IO-pin of the VME chip is connected to a tri-state driver and an input buffer to sense also the status of the Virtex-II chip after releasing the driver. The PWRDWN bit in the status register of the VME chip reflects the state of the Virtex-II chip.

(From the *Virtex-II User Guide.)*
The power-down sequence enables a designer to set the device into a low-power, inactive state. The sequence is initiated by pulling the PWRDWN_B pin Low. The BitGen PWRDWN_STAT option is no longer supported. To monitor power-down status, observe the PWRDWN_B pin. When asserted, power-down has completed. After a successful wake-up, the status pin de-asserts. While powered down, the only active pins are the PWRDWN_B and DONE. All inputs are off and all outputs are 3-stated. While in the POWERDOWN state, the Power On Reset (POR) circuit is still active, but it does not reset the device if VCCINT, VCCO or VCCAUX falls below its minimum value. The POR circuit waits until the PWRDWN_B pin is released before resetting the device. Also, the PROG_B pin is not sampled while the device is in the POWERDOWN state. The PROG_B pin becomes active when the PWRDWN_B pin is released. Therefore, the device cannot be reset while in the POWERDOWN state. The wake-up sequence is the reverse of the power-down sequence.

8.7.3 Maximum input voltage =+3.6V

Never higher than 4.0 V !!!

8.7.4 Termination Resistors

The VirtexII chip contains DCI circuits to control the impedance of the io-pins digitally. This property saves many termination resistors on the board and avoids stubs on terminated nets. For each bank a pair of resistors

that is connected to VCCO=3.3V and GND, is used as reference for the termination. The DCI function is enabled in the TIM chip design for each io-pin individually.
The pins VRN are connected over R=50 Ohm 1% to VCCO=3.3V and the VRP pins are connected over R=50 Ohm, 1% to GND.

8.7.5 Hot Swap Enable

(From the *Virtex-II User Guide.)*
Prior to configuration, all outputs not involved in configuration are forced into their high-impedance state. The pull-down resistors and the weak-keeper circuits are inactive. The dedicated pin HSWAP_EN controls the pull-up resistors prior to configuration. By default, HSWAP_EN is set high, which disables the pull-up resistors on user I/O pins. When HSWAP_EN is set low, the pull-up resistors are activated on user I/O pins.
(From the *Virtex-II User Guide pg.81)*
Depending on the system design, several configuration modes are supported, selectable via mode pins. The mode pins M2, M1 and M0 are dedicated pins. An additional pin, HSWAP_EN is used in conjunction with the mode pins to select whether user I/O pins have pull-ups during configuration. By default, HSWAP_EN is tied High (internal pull-up) which shuts off the pull-ups on the user I/O pins during con-figuration. When HSWAP_EN is tied Low, user I/Os have pull-ups during configuration.
TIM board:
The signal HSWAP_EN is connected on the board to a jumper to connect HSWAP_EN to GND to enable the internal pull-up resistors during configuration. If the jumper is removed (=default) the pull-up resistors are disabled during configuration as described above.

9 JTAG

TDI-TDO chain: Insert a jumper for each chip to remove it from the chain if necessary.

There are some questions with the JTAG chains on board which have to be discussed:

- How many chains on board?
- What to do with TTCrx JTAG chain?
- How to implement the JTAG solution of DTTF-crate which is made by VMEbus?

10 Front panel

TO BE DEFINED!!!!

On the front panel there are the following components arranged:

10.1 LEDs

- Red LED as indicator that the module is in an INACTIVE state, ready for removal.
- Green LED for RUNNING state, module is able to run in the specified meaning.
- INACTIVE and RUNNING LED should be placed near „Interlock“-switch on the top of front panel.
- Red LED for TTCRX_ERR, indicator of errors on the TTCrx-board. This signal is a status or a pulse ????? Where to place??
- Green LED for TTCREADY. This signal is a status or a pulse ????? Where to place??
- Red LED for L1ACCEPT. How long should to pulse be for LED ??????? Where to place??
- Green LED for VMEbus-access. VME_LED signal out of VME-chip indicates a VMEbus-access to the module (AS* is active) ??????? How long should to pulse be for LED ?? Where to place??

10.2 Switches

- „Interlock“-switch forces the module in INACTIVE/RUNNIG state. Should be placed on the top of the front panel.
- CLK_LEMO-switch selects CLOCK40DES1 or LOCAL_CLK to lemo-connector. Where to place??

- LOCAL_CLK-switch selects oszillatorclock or external clock to LOCAL_CLK. Where to place??
- SEL_TTCLK-switch ???????????. Where to place??

10.3 LEMO-connectors

- LEMO-outputs for 8 clock signals (CKO1..8), level 1 accept signal (L1A_TTC), bunch counter reset signal (BCRES_TTC) and a reset signal (RESET_TTC) from TTCrx board. Where to place??
- The source for the 8 clock output signals can be selected by jumpers.
- Another LEMO output is used to monitor either the TTCrx or the Oscillator clock signal, that has been selected by a front panel switch.
- LEMO-inputs of external clock signal (CLK_X), external level 1 accept signal (L1A_X), external bunch counter reset signal (BCRES_X) and an external reset signal (RESET_X). Where to place??
- Remark: The ABTE16245 have been selected as 50 Ohm drivers and provide +90/-60 mA. The 25 Ohm resistors at the B-side of the ABTE16245 reduce under/overshoot of the signals. Therefore no other termination resistors are foreseen between the LEMO output driver and the clock sources.
- Optical-link to/from TTCrx-board
- The TTCrx-board is placed near the front of the module so that the optical-link-connector is connectable.

11 Hot Swap

The TIM-card is designed to work in a hot-swap-system. There are made a set of precaution to prevent damages or incorrect behaviours of the used devices.
Two push-buttons on the front panel are forseen to set the module in a defined state to handle with it. Inserting the module in a powered system is possible because all drivers are disabled with the INACTIVE signal, which is generated at powerup of VCCBIAS, which is supplied with staged length contact of the 160 pin VME64 connector (D32). All the devices which generate the enable signals for the drivers to the backplane are supplied with VCCBIAS or LV3V3BIAS. LV3V3BIAS is made from VCCBIAS (D1) when used in the system with the 6U-backplane. In the 9U-backplane LV3V3BIAS will be supplied on a staged length contact of the 160 pin VME64 connector (D1).
Inserting the module in a powered crate keeps the module in the INACTIVE state until the RUNNUNG push-button is pressed. If the module is inserted in a unpowered crate, after powerup the INACTIVE state is set, but the RUNNING state is set with signal SET_RUNNING which is generated in the VME chip by VMEbus SYSRES*.
Removing the module from a powered system is made by pressing the INACTIVE push-button to set the module in an INACTIVE state which disables the drivers and remove the module from crate.
The INACTIVE and RUNNING states are indicated with leds.

The definitions of the hot-swap-system for GT-crate modules are written in the file GT_liveinsertion.doc.- ALTE VERSION!!!

11.1 VME64 connector 160 pins

The connector contains 4 leading pins D1, D32 for +5V and D2, D31 for GND.

11.2 VMEbus buffer driver SN74ABTE16245DL

The A port is foreseen for the VMEbus side (I_{OH}=-60mA, I_{OL}=90mA, 25 Ohm incident wave switching).

- Internal pull-up resistor on OE keeps outputs in high-impedance state during power up or power down.
- V_{CC} BIAS pin minimizes signal distortion during Live Insertion.

Live Insertion SDYA012.pdf from Texas Instruments:
The ETL circuits (for example, SN74ABTE16245) have an additional supply voltage connection (V_{CC} BIAS). This feeds the circuit, which generates the voltage bias mentioned above and, together with the V_{CC} connection, controls the switching on and off of the voltage bias. Figure 12 shows the simplified circuit diagram of this part of the circuit. It does not include the power-up 3-state circuit (see Figure 2), which also is contained in these bus interface circuits, and which switches all outputs into the high-impedance state (3-state) at a supply voltage below about 2.5 V.
TIM board:
The leading +5V voltage pins are connected to the VCCBIAS pin of the ABTE16245. It's /OE pin is controlled by the INACTIVE signal.

11.2.1 Interlock Switch

The interlock switch is made of two push-buttons one to setting the module INACTIVE and one to set it RUNNING.Functionality in a powered system:

Insertion
Insert the module → INACTIVE state, all drivers disabled
Push RUNNING button → RUNNING state, all drivers enabled
Removing
Push INACTIVE button → INACTIVE state, all drivers disabled
Remove the module

Functionality in an unpowered system:

powerup → INACTIVE state, all drivers disabled
with SYSRES* → SET_RUNNING signal, RUNNING state, all drivers enabled

11.3 VME chip

The VME chip does not drive directly any VMEbus signals. Until the end of configuration all IO-pins are in high impedance state. No special protection is foreseen.

11.4 DTACK and BERR driver 74F38

The open collector outputs of the 74F38 are insensitive to high voltage levels as long as they are below +7 Volt. No protection is necessary for live insertion. Moreover the outputs are kept inactive by INACTIVE signal.

11.5 LVDS drivers SN75LVDS387

The SN75LVDS387 drive point-to-point lines. Therefore no bus problems arise. The drivers are in high impedance state until the TIM chip has been configured. Before removing the board their outputs are locked to high impedance by the interlock switch via the TIM chip.
When not powered up the outputs of the SN75LVDS387 see only differential inputs of LVDS receivers.

11.6 Signal driver ABT18245

The ABT18245 drive point-to-point lines. Therefore no bus problems arise. The drivers are in high impedance state until the TIM chip has been configured. Before removing the board their outputs are locked to high impedance by the interlock switch via the TIM chip.
When not powered up the ABT18245 outputs are insensitive against voltage levels below 7 Volt.

11.7 MOS-FET swich 74CBTLV16800

This device is used to isolate signals from the backplane, which are driven from the Virtex-chip.

11.8 TIM chip Virtex-II XC2V1000FG456-4

Voltages more than +0.7V higher than the actual VCCOUT level can destroy Virtex-II pins because of the diode from the pin to VCCOUT. Therefore no IO-pin of the Virtex-II chip is connected to the back-plane to protect the chip during live insertion. The connection to +5V devices like ABT18245 is made with a serial R of 50Ω.

See XAPP251 Hot-Swapping Virtex-II Devices from Xilinx.
Each IO-pin contains a diode from pin to VCCO and from GND to pin.
In the best case, ground and VCC pins mate first and the VCC distribution on the board feeds all the positive supply pins before any signal pins mate. When the on-board VCC distribution is slow and signal pins mate before the supply voltage is completely powered, then any active High signal pin might drive current through the diode into the VCC pin.

11.9 JTAG

JTAG signals are isolated from the backplane with a 74CBT3245A device.

11.10 Hot swap questions

ESD
IACK IN-OUT on VMEbus

11.11 Clock Signals on 6U-Backplane

TimCard	Backplane	Slot
L1	GTL2	14
L2	GTL1	13
L3	PSB6	12
L4	PSB5	11
L5	PSB4	10
L6	PSB3	9
L7	GMU1	7
L8	PSB1	5
R1	FDL1	16
R2	FDL2	17
R3	GTFE	18
R4	GTL3	19
R5	PSB7	20
R6	PSB8	21
R7	GMU2	8
R8	PSB2	6