CSC – GMT Test report

H. Sakulin, A. Taurok

Vienna, 31 January 2005

We tested the data interface between he CSC Muon Sorter and the Global Muon Trigger board and measured a bit error rate less than 10^{-13} bit/s sending a set of pseudo random data repeately.

1 Test setup

The CSC crate contained a VME-bus controller SBS620, a Clock and Control board (CCB) with a TTCrm mezzanine board and the Muon Sorter board (MS).

The GT configuration consisted of a SBS620 VME controller, a Timing board (TIM6U) with a TTCrm mezzanine board and the Global Muon Trigger (GMT) board. Additionally, a TTCvi board was mounted in the GT crate in order to create periodic bunch-counter reset signals. Both crates were controlled by Linux-PCs.

A TTCex board was mounted in a standard VME-6U crate. The internal 40.08 MHz clock signal of the TTCex board was taken as the only clock source of the test setup and connected to the CLOCK IN (ecl) input of the TTCvi that was programmed to send a BCReset signal every 3564th bunch crossing back to the TTCex, simulating LHC orbits. The clock and the BCReset signal were then transmitted to the GMT and the CSC timing/clock boards via the optic outputs of the TTCex board.

The TIM6U board in the GT crate was programmed to forward the 40 MHz clock and the BCReset signal via the back-plane to the GMT board.

The Muon data were sent via shielded, halogenfree cables containing 34 twisted pairs. The cable length has been 11m, slightly longer than the expected maximum length.

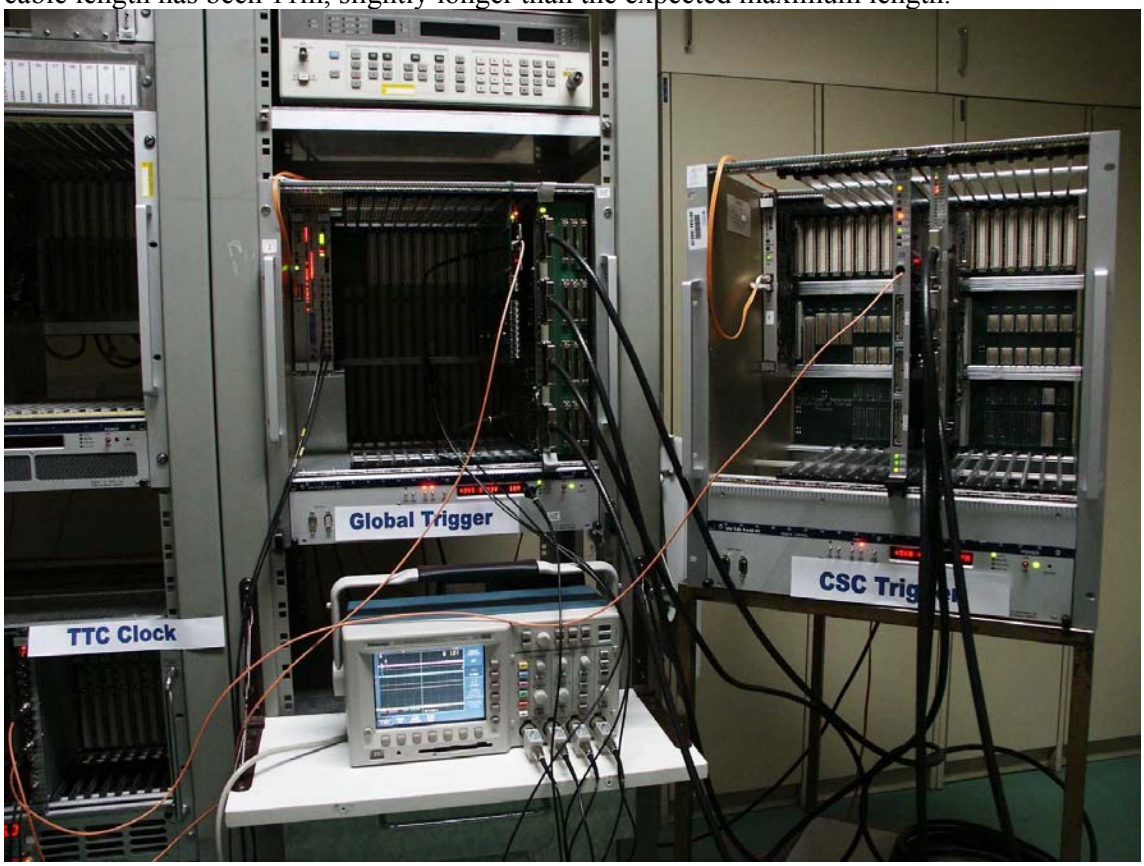

Figure 1 Test setup

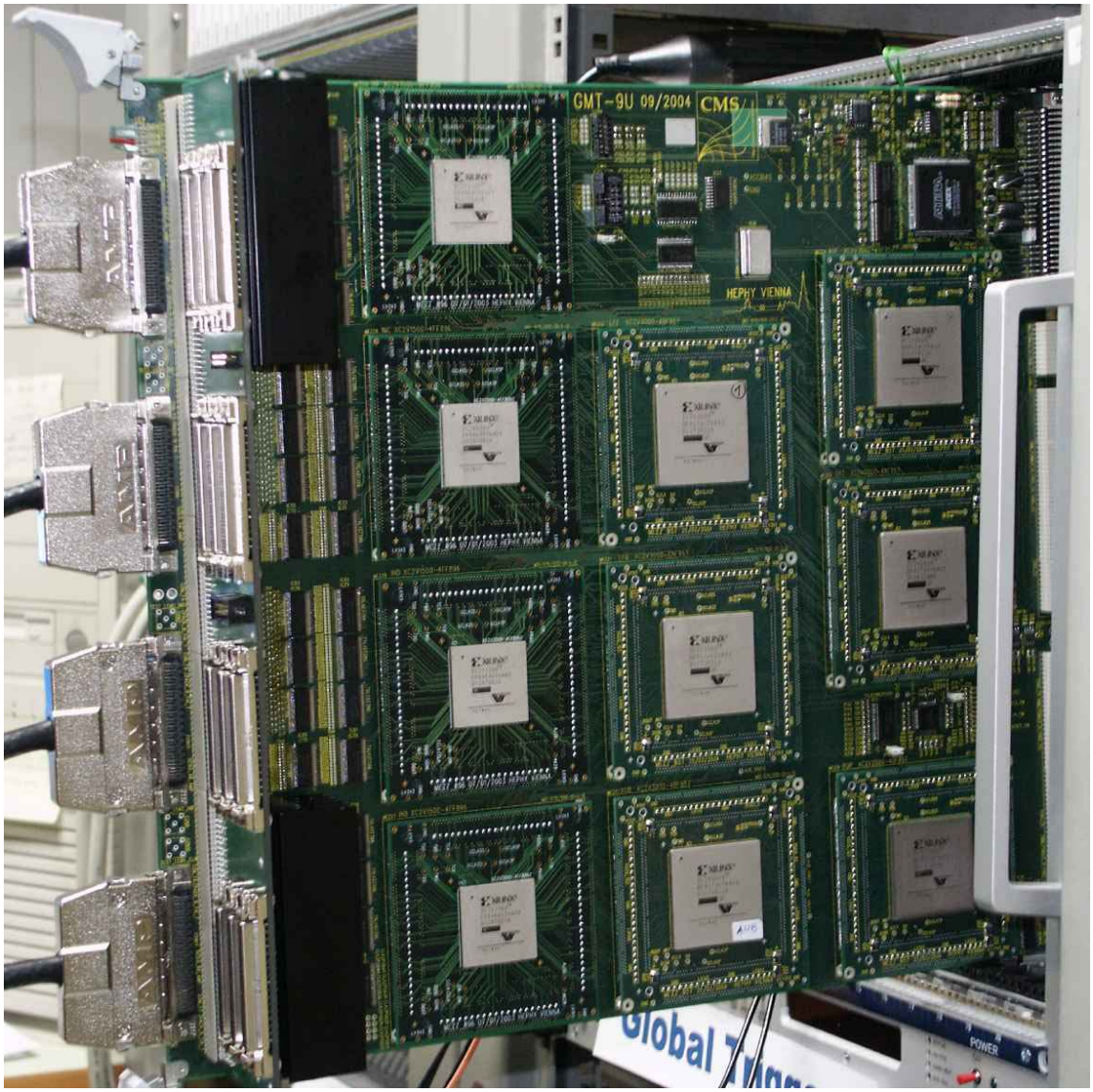

Figure 2 Global Muon Trigger board

2 Differential signals

The CSC-MS memory was loaded with a 'running one' pattern to check if the MS sends data correctly as LVDS signals via shielded TP cables. We found that we have to use the internal MS oscillator as clock source to load the data correctly into the MS memory. Then we switched to the common TTC clock to send the memory data to the GMT that was always running with the common TTC clock.
At the receiver side the amplitude of the LVDS signals was +/- 350 mV giving a differential voltage of about 700 mV. We saw small reflections because of small impedance differences between the cable and the input connectors and because of the internal termination resistors (~105 Ohm) of the 75LVDT386 receiver chips. See also Figures 3 and 4.

3 Oversampling of input signals

Input circuit of the GMT:

To find the switching time of the input data the input chips of the GMT samples each bit 4 times per bunch crossing. Four XOR functions between two consecutive samples

of the bit 0 signal increment 4 ‘phase’ counters showing at which time input bits change their level.

Result:

Only one counter was incremented showing that the input bit 0 switches always between these two sampling times and that both systems are stable in time to each other.

We selected the other two sampling times to store the data. We could also select a third sampling time without getting errors, because the switching time was close to one sampling time and the signal rise and fall times were very small in the order 2 ns.

4 Test with ‘running 1’ pattern

The MS memories were loaded with a ‘running 1’ test pattern (0001 0001, 00020002, 00040004 …80008000). See also screenshot of the oscilloscope in Figure 4 showing the differential signal of one data bit at the GMT connector pin.

Remark1:

When using the TTC clock wrong data patterns were loaded into the MS memories as can be seen in Figure 3. Therefore we used the MS-internal clock to load the memories. Then we switched back to the TTC clock to send the data to the GMT.

In the GMT input chips additional logic was implemented to compare the input data with the data stored in the SPY/SIM memory. For each input bit also an error counter was added.

First, data of one orbit were stored as reference in the SPY memories. Then the memories were switched into ‘SIMULATION’ mode and the following data were compared against the reference values and any difference incremented the error counters.

Both, the CSC as well as the GMT memory readout were synchronized by the BCReset signal broadcasted via the TTC system.

We connected 4 cables to the muon0 inputs of the 4 input groups (CSC, DT, RPCfwd, RPCbrl) and did not see any error during several hours. Then we connected the 4 cables to the 4 CSC inputs of the GMT and also did not observe any error running the system overnight for 12 h.

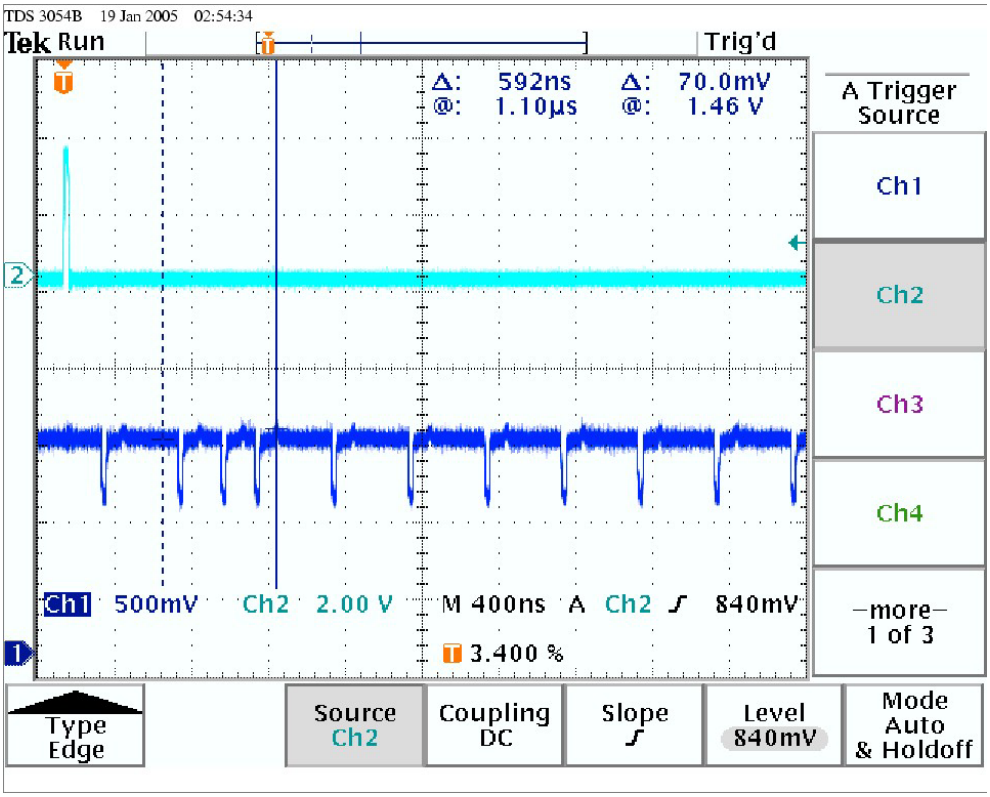

Figure 3: ‘Running-1’ pattern with bad data bits

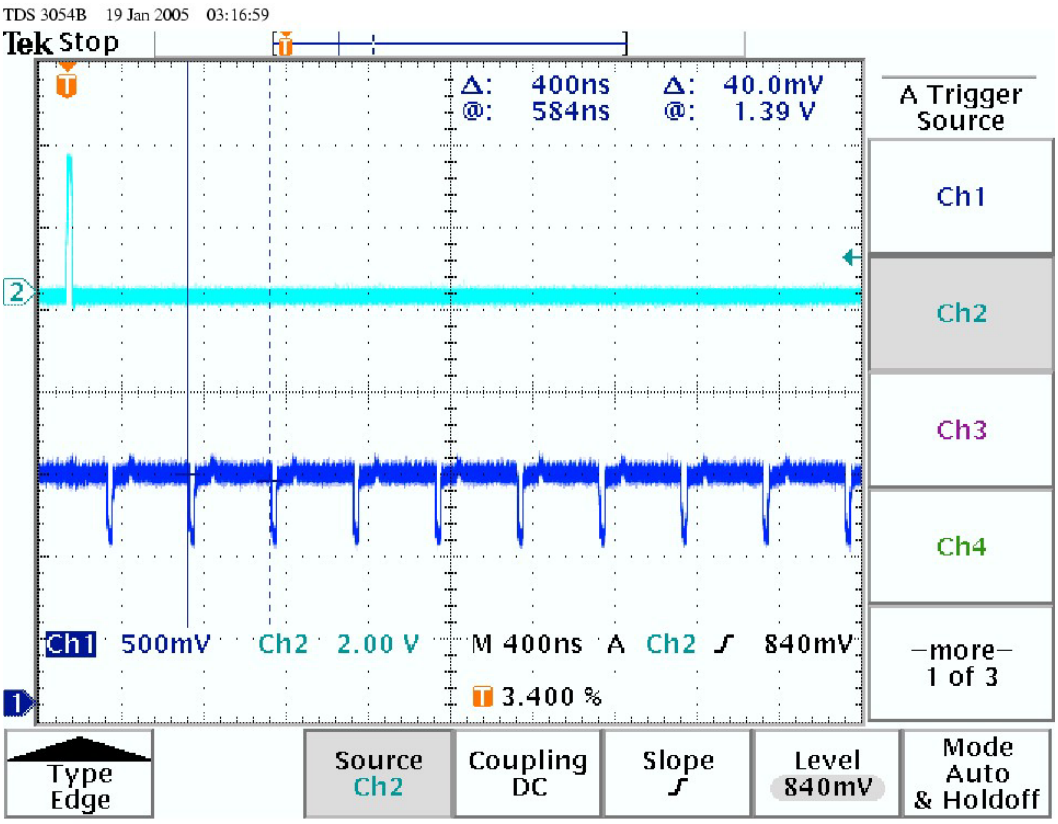

Figure 4: 'Running-1' pattern without errors

5 Test with random data

Five hundred locations in the Muon Sorter CSC-MS memory were loaded with random data. As described above the data of the first orbit were stored as reference. The transfer of data was running for 16 hours sending about 3,84 x 10^{13} bits to the GMT and no error was observed.

Calculation:

500 words x 4muons x 30 bits within 90 us (1 orbit) ➔ *3,84 x 10^{13} bits within 16 hours.*

Therefore the bit error rate for the CSC to GMT link is less than 10^{-13} errors/s running in an laboratory environment.