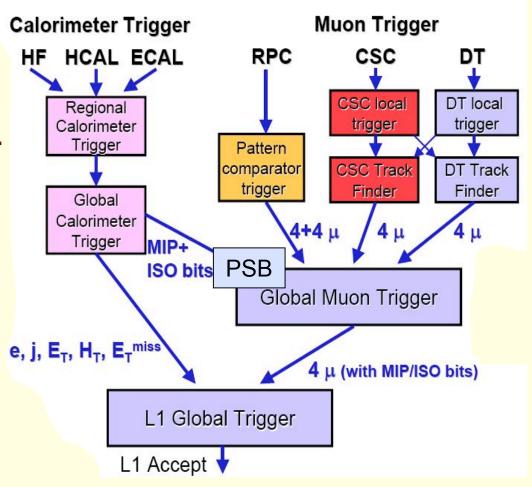
Integration tests with Global Muon Trigger

Tobias Nöbauer and Ivan Mikulec HEPHY Vienna

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Overview

- GMT Self-tests
- GMT Integration tests
 - Test with PSB
 - Test with DTTF
 - Test with CSCTF
- SW activities
- Conclusions

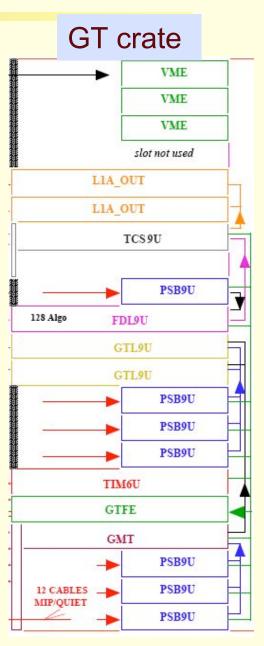


GMT Self-tests

- Self-tests of the GMT module were done in Vienna using ORCA data (H→ZZ→4µ)- full internal functionality reproduced (apart from 4 bit errors - 2 corrected in the firmware)
- Mid-December GMT module arrived at CERN
- Before Christmas self-tests were repeated in b. 904
- From the beginning of January GMT was ready for integration

Test with PSB

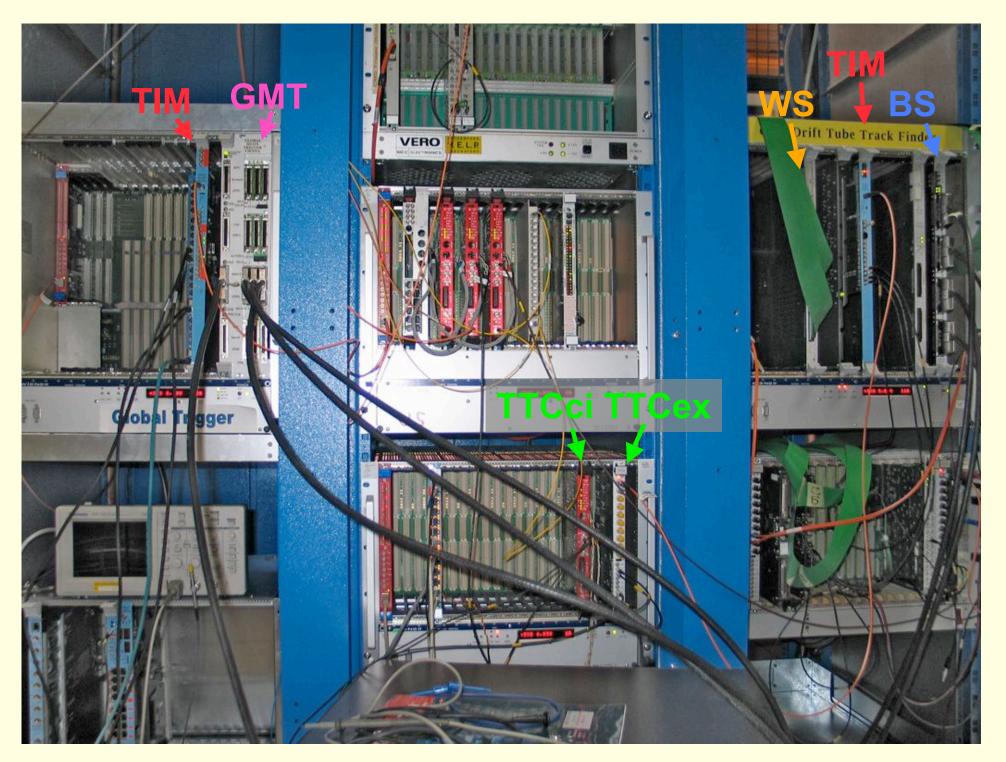
- PSB (Pipelined Synchronising Buffer) synchronises the GCT inputs into GT and GMT
- Only one PSB board available at CERN for the moment (3 PSBs foreseen for the GMT input)
- Test was done using special ORCA data:
 - modified to account for one PSB only
 - MIP/ISO information written into the PSB board
 - Muon inputs written into GMT simulation memories in the input FPGA's
 - Timing (clock and BCreset) provided by the GT TIM module
- After a fine timing adjustment, data were received and combined by the GMT correctly
- A couple of transmission bit errors found
- Tobias is preparing new test firmware to localise these bit errors

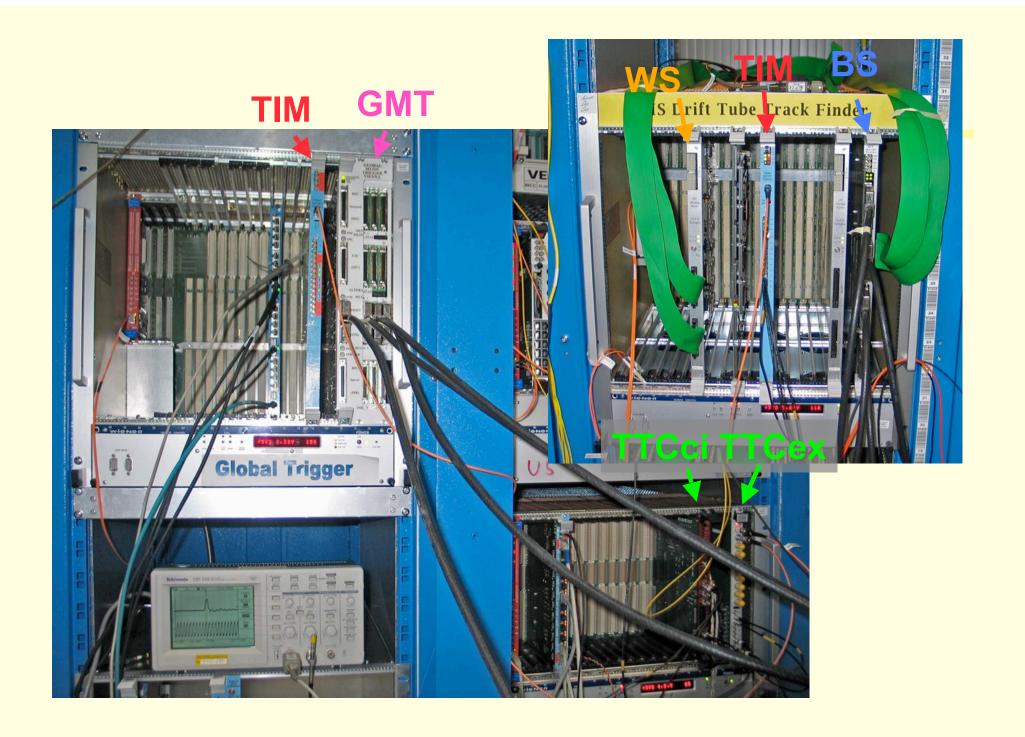


Test with DTTF

- In collaboration with Janos
- Bit patterns sent from Wedge Sorter (WS) through Barrel Sorter (BS) into GMT
- Common clock provided by TTCci and split by TTCex (thanks to Jan for his assistance) and received by TIM modules in both crates
- All 16 GMT input connectors were scanned (4 bit errors in total found on the GMT side)
- Next step is to try to connect more modules in a chain and use ORCA data

I. Mikulec: GMT Integration





Test with CSCTF

- Mid-January the new CSC Muon Sorter board (MS2005) arrived at CERN
- Dan installed it in the CSCTF crate
- It was self-tested remotely by Sang-Joon Lee from Rice
- Our interconnection test was synchronised using TTCci/TTCex system connected to TIM board in the GT crate and CCB (Clock and Control Board) in the CSCTF crate:
 - Test pattern was written into MS RAMs
 - The transmission was triggered by a BC0 broadcast from TTCci
 - The same signal triggered reading of spy memories in the GMT input FPGA
 - Data were aligned for comparison with appropriate delay
- No problems have been found

I. Mikulec: GMT Integration







SW activities

- On the fly development of test SW for the integration activities in b. 904
- New firmware with updated LUTs
- Test firmware for MIP/ISO FPGas
- Integration to Trigger Supervisor
- Configuration database

Layout of the GMT config. db

GMT_FIRMWARE

FW_KEY_VARCHAR2(32) NOT NULL (PK) VERSION NUMBER(32) NULL URL VME VARCHAR2(512) NULL URL_JAL_VARCHAR2(512) NULL URL_BYTEBLASTER VARCHAR2(512) NULL DESCRIPTION VARCHAR2(512) NULL

GMT_INX_REGISTERS

IF_REG_KEY_VARCHAR2(32) NOT NULL (PK) IF_SYNCCONFIGREG_ADDRO NUMBER(5) NULL IF_SYNCCONFIGREG_ADDR1_NUMBER(5) NULL IF_SYNCCONFIGREG_ADDR2 NUMBER(5) NULL IF_SYNCCONFIGREG_ADDR3_NUMBER(5) NULL IF_READOUTSYNCREG_ADDR_NUMBER(5) NULL IF_LATDELAYREG_ADDR_NUMBER(5) NULL IF_SIMUSPYCONFIG_ADDR_NUMBER(5) NULL IF_SPYDEPTH_ADDR_NUMBER(5) NULL IF_SPYARMPULSE_WADDR_NUMBER(5) NULL IF_COMPARECOUNTERRESET_WADDR_NUMBER(5) NULL DESCRIPTION VARCHAR2(512) NULL

GMT_LFX_REGISTERS

LF_REG_KEY VARCHAR2(32) NOT NULL (PK) LF_CDLCONFIG_ADDRO_NUMBER(5) NULL LF CDLCONFIG ADDR1 NUMBER(5) NULL LF_SORTRANKOFFSET_ADDR_NUMBER(5) NULL LF_MMCONFIG_SRK_ADDR_NUMBER(5) NULL LF_MMCONFIG_PHI_ADDR_NUMBER(5) NULL LF_MMCONFIG_ETA_ADDR_NUMBER(5) NULL LF_MMCONFIG_PT_ADDR_NUMBER(5) NULL LF_MMCONFIG_CHARGE_ADDR_NUMBER(5) NULL LF_MMCONFIG_MIP_ADDR_NUMBER(5) NULL LF_MMCONFIG_ISO_ADDR_NUMBER(5) NULL DESCRIPTION VARCHAR2(512) NULL

GMT_SRT_REGISTERS

SF_REG_KEY_VARCHAR2(32) NOT NULL (PK) SF_READOUTSYNCREG_ADDR_NUMBER(5) NULL SF_LATDELAYREG_ADDR_NUMBER(5) NULL SF_SIMUSPYCONFIG_ADDR_NUMBER(5) NULL SF_SPYDEPTH_ADDR_NUMBER(5) NULL SF_SPYARMPULSE_WADDR_NUMBER(5) NULL DESCRIPTION VARCHAR2(512) NULL

GMT_CONFIG

GMT_KEY_VARCHAR2(32) NOT NULL (PK) INB_FW_KEY VARCHAR2(32) NOT NULL (FK) INB_REG_KEY VARCHAR2(32) NOT NULL (FK) INC_FW_KEY_VARCHAR2(32) NOT NULL (FK) INC_REG_KEY VARCHAR2(32) NOT NULL (FK) IND_FW_KEY_VARCHAR2(32) NOT NULL (FK) IND_REG_KEY_VARCHAR2(32) NOT NULL (FK) INF_FW_KEY_VARCHAR2(32) NOT NULL (FK) INF_REG_KEY_VARCHAR2(32) NOT NULL (FK) AUF_FW_KEY VARCHAR2(32) NOT NULL (FK) AUF_REG_KEY_VARCHAR2(32) NOT NULL (FK) AUF_LUTS_KEY VARCHAR2(32) NOT NULL (FK) AUB_FW_KEY VARCHAR2(32) NOT NULL (FK) AUB_REG_KEY VARCHAR2(32) NOT NULL (FK) AUB LUTS KEY VARCHAR2(32) NOT NULL (FK) LFF_FW_KEY VARCHAR2(32) NOT NULL (FK) LFF_REG_KEY VARCHAR2(32) NOT NULL (FK) LFF_LUTS_KEY_VARCHAR2(32) NOT NULL (FK) LFB_FW_KEY_VARCHAR2(32) NOT NULL (FK) LFB_REG_KEY_VARCHAR2(32) NOT NULL (FK) LFB_LUTS_KEY VARCHAR2(32) NOT NULL (FK) SRT_FW_KEY_VARCHAR2(32) NOT NULL (FK) SRT_REG_KEY_VARCHAR2(32) NOT NULL (FK) ROP_FW_KEY_VARCHAR2(32) NOT NULL (FK) ROP_REG_KEY_VARCHAR2(32) NOT NULL (FK) DESCRIPTION VARCHAR2(512) NULL

GMT_ROP_REGISTERS

ROP_REG_KEY_VARCHAR2(32) NOT NULL (PK) ROP_RESET_ADDR_NUMBER(5) NULL ROP_RESET_DCM_ADDR_NUMBER(5) NULL ROP_COMMAND_ADDR_NUMBER(5) NULL ROP_TAG_ENABLE_ADDR_NUMBER(5) NULL ROP_PROG_ENABLE_ADDR_NUMBER(5) NULL ROP_NPROG_ADDR_NUMBER(5) NULL ROP_INIT_CMD_ADDR_NUMBER(5) NULL ROP_DIN_INF_ADDR_NUMBER(5) NULL ROP_DIN_INC_ADDR_NUMBER(5) NULL ROP_DIN_IND_ADDR_NUMBER(5) NULL ROP_DIN_INB_ADDR_NUMBER(5) NULL ROP_DIN_AUF_ADDR_NUMBER(5) NULL ROP_DIN_LFF_ADDR_NUMBER(5) NULL ROP_DIN_LFB_ADDR_NUMBER(5) NULL ROP_DIN_AUB_ADDR_NUMBER(5) NULL ROP_DIN_SRT_ADDR_NUMBER(5) NULL ROP_DUMMY_CMD_ADDR_NUMBER(5) NULL ROP_LATDELAYREG_ADDR_NUMBER(5) NULL ROP_VMEWRITEALLMASK_ADDR_NUMBER(5) NU DESCRIPTION VARCHAR2(512) NULL

GMT_AUX_REGISTERS

MIAU_REG_KEY_VARCHAR2(32) NOT NULL (PK) MIAU_READOUTSYNCREG_ADDR_NUMBER(5) NULL MIAU_SIMUSPYCONFIG_ADDR_NUMBER(5) NULL MIAU_SPYDEPTH_ADDR_NUMBER(5) NULL MIAU_SPYARMPULSE_WADDR_NUMBER(5) NULL DESCRIPTION VARCHAR2(512) NULL

GMT_LFX_LUTS

LF_LUTS_KEY_VARCHAR2(32) NOT NULL (PK) LF_MATCHQUALLUT_BASE0 VARCHAR2(512) NULL LF_MATCHQUALLUT_BASE1 VARCHAR2(512) NULL LF_MATCHQUALLUT_BASE2 VARCHAR2(512) NULL LF_COUDELTAETALUT_BASE0 VARCHAR2(512) NULL LF_COUDELTAETALUT_BASE1 VARCHAR2(512) NULL LF_OVLETACONVLUT_BASEO_VARCHAR2(512) NULL LF_OVLETACONVLUT_BASE1 VARCHAR2(512) NULL LF_OVLETACONVLUT_BASE2_VARCHAR2(512) NULL LF_ETACONVLUT_BASEO VARCHAR2(512) NULL LF_ETACONVLUT_BASE1 VARCHAR2(512) NULL LF_MERGERANKPTQLUT_BASE0_VARCHAR2(512) NULL LF_MERGERANKPTQLUT_BASE1_VARCHAR2(512) NULL LF_PHIPROETACONVLUT_BASE0_VARCHAR2(512) NULL LF_PHIPROETACONVLUT_BASE1 VARCHAR2(512) NULL LF_BLOCKRAM_BASE VARCHAR2(512) NULL LF_SORTRANKETAQLUT_BASEO VARCHAR2(512) NULL LF_SORTRANKETAQLUT_BASE1 VARCHAR2(512) NULL LF_SORTRANKPTQLUT_BASE0 VARCHAR2(512) NULL LF_SORTRANKPTQLUT_BASE1 VARCHAR2(512) NULL LF_SORTRANKETAPHILUT_BASEO VARCHAR2(512) NULL LF_SORTRANKETAPHILUT_BASE1 VARCHAR2(512) NULL LF_SORTRANKCOMBINELUT_BASE0 VARCHAR2(512) NULL LF_SORTRANKCOMBINELUT_BASE1 VARCHAR2(512) NULL LF_DELTAETALUT_BASE0 VARCHAR2(512) NULL LF_PTMIXLUT_BASEO VARCHAR2(512) NULL LF_MERGERANKETAQLUT_BASEO VARCHAR2(512) NULL LF_MERGERANKETAQLUT_BASE1 VARCHAR2(512) NULL LF_MERGERANKETAPHILUT_BASEO_VARCHAR2(512) NULL LF_MERGERANKETAPHILUT_BASE1 VARCHAR2(512) NULL LF_MERGERANKCOMBINELUT_BASEO VARCHAR2(512) NULI LF_MERGERANKCOMBINELUT_BASE1 VARCHAR2(512) NULL LF_DISABLEHOTLUT_BASE0_VARCHAR2(512) NULL LF_PHIPROLUT_BASEO VARCHAR2(512) NULL LF_PHIPROLUT_BASE1 VARCHAR2(512) NULL DESCRIPTION VARCHAR2(512) NULL

GMT AUX LUTS

MIAU_LUTS_KEY VARCHAR2(32) NOT NULL (PK) MIAU_ETACONVLUT_BASE0 VARCHAR2(512) NUL MIAU_ETACONVLUT_BASE1 VARCHAR2(512) NUL MIAU_ETACONVLUT_BASE2_VARCHAR2(512) NUL MIAU_ETACONVLUT_BASE3 VARCHAR2(512) NUL MIAU_PHIPRO1LUT_BASE0 VARCHAR2(512) NULL MIAU_PHIPRO1LUT_BASE1 VARCHAR2(512) NULL MIAU_PHIPRO1LUT_BASE2 VARCHAR2(512) NULL MIAU_PHIPRO1LUT_BASE3 VARCHAR2(512) NULL MIAU_PHIPRO2LUT_BASE0 VARCHAR2(512) NULL MIAU_PHIPRO2LUT_BASE1 VARCHAR2(512) NULL MIAU_PHIPRO2LUT_BASE2 VARCHAR2(512) NULL MIAU_PHIPRO2LUT_BASE3 VARCHAR2(512) NULL MIAU_ETAPROLUT_BASE0 VARCHAR2(512) NULL MIAU_ETAPROLUT_BASE1 VARCHAR2(512) NULL MIAU_ETAPROLUT_BASE2 VARCHAR2(512) NULL MIAU ETAPROLUT BASES VARCHAR2(512) NULL DESCRIPTION VARCHAR2(512) NULL

Conclusions

- Integration tests of several trigger chains leading to the GMT have been started in parallel in the integration area of b. 904
- TTCci/TTCex system has been installed and tested in the integration area as a basic synchronisation tool for these tests
- The RPC chain can be tested as soon as RPC electronics is ready (end of February?)
- Tests with DTTF and CSCTF will continue by adding new elements to the chain and using ORCA simulation to calculate the expected response