

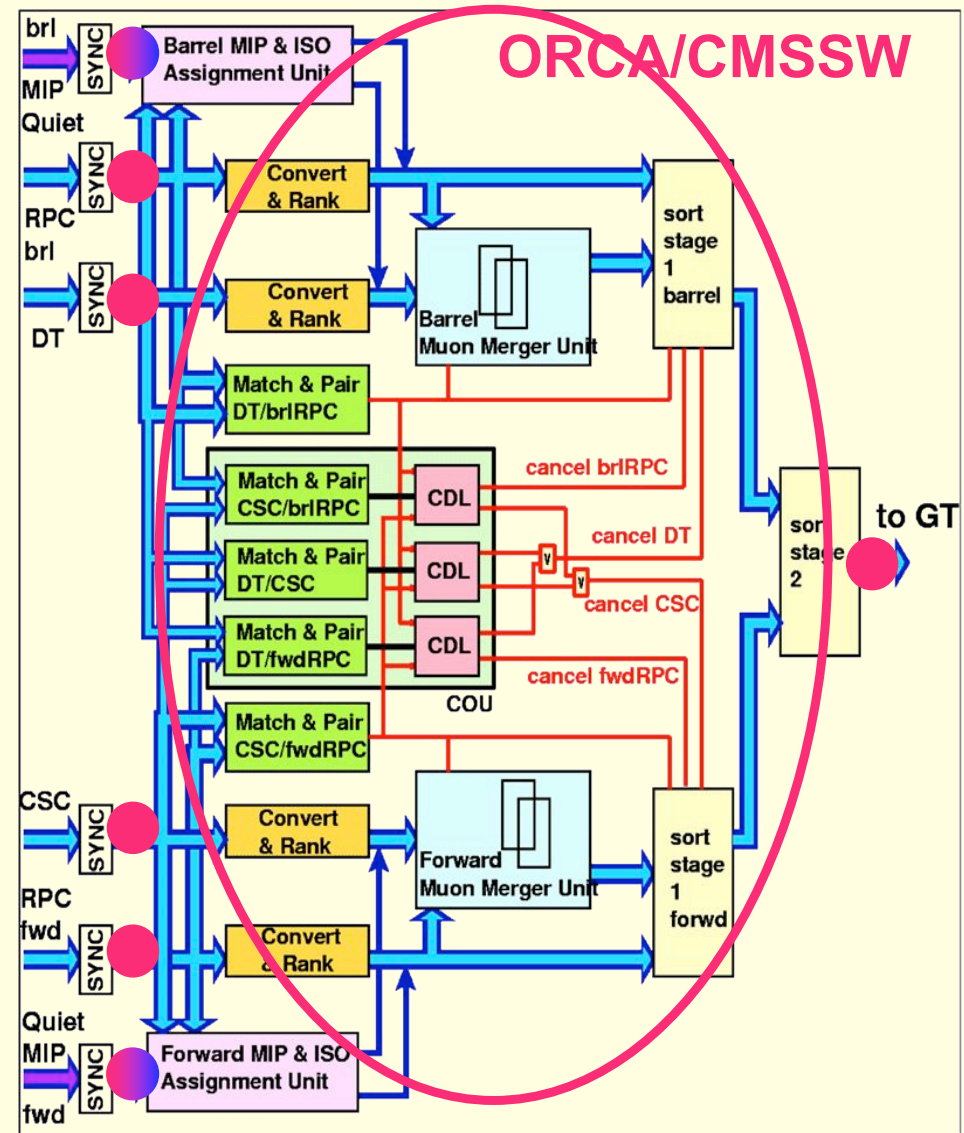
Integration tests with Global Muon Trigger

Ivan Mikulec
HEPHY Vienna

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Testing capabilities in GMT

- **Simulation** and **spy** memories are embedded in the firmware of **Input** and **Sorter** FPGA's.
- **Real time bit-error counting** (at each orbit spy memory content of Input FPGA's is compared to the content of the first orbit)
- **Optional** firmware for **MIP&ISO** Assignment units contains **spy** memories (load by VME)
- **ORCA** simulation has **emulator** capability - input and output can be generated and compared bit by bit (starting to migrate to **CMSSW**)



- simu/spy standard
- simu standard, spy optional

RPC-GMT interconnection test

- During March, the connection between the **Final Sorter of the RPC** trigger to the **GMT** has been tested
- Common TTCci/TTCex clock and command source
- Transmission from the Sorter and reading at GMT of patterns started with BC0
- The **real time bit error counting on 4 inputs** showed **no error** after 16h which corresponds to **>6x10¹³ bits** (16h x 4 x 1024 words/orbit x 24 bits).
- Plans are to connect more modules at the upstream side as soon as RPC ready.

GMT-GTL test

- All components of a **second GMT module** are ready and tested in Vienna
- It is **being assembled** now
- An interconnection test between **GMT** and **GTL** will be performed in Vienna in next week(s)
- A feature that allows a **collective read-out** of all spy memories in the **GMT/GT system** is under preparation (should be ready for cosmic challenge)

Conclusions

- The **RPC-GMT** connection has been tested successfully.
- All input connections to the GMT board have been by now tested in b. 904 (DTTF-GMT, CSCTF-GMT, RPC-GMT, PSB-GMT).
- **Second GMT module** will be available soon.
- The output connection **GMT-GTL** will be tested in Vienna with this second module.
- We are preparing for **MTCC** (collective GMT/GT spy read-out, TS integration)
- We will move our equipment to P5 during May