Global Muon Trigger Module

9U-Version

H. Bergauer, M. Padrta, H. Sakulin, A. Taurok

3 Common logic circuits

3.1 Configuration of FPGAs and Proms

Standard configuration modes:
1) Normally all FPGA chips are configured at Power-Up by the content of the PROMs. Therefore all FPGAs are soldered to run in MASTER SERIAL mode during configuration from Proms. *(Solder SMD-resistors on the MEZZ896 board to set M2=M1=M0=LOW ➔ MASTER MODE).*
2) New permanent versions are loaded into the PROMs by VME-JTAG with only the PROMs included into the JTAG-chain. *This method cannot configure the VME64 chip.*
3) The Altera Byte Blaster has to be used to load a new permanent version for the VME64 chip.
Optional configuration modes for tests:
1) To load a new temporary version for tests the FPGA chips (INB, INC, IND, INF, LFB, LFF, AUB, AUF, SRT) can be reconfigured directly via VME-JTAG but then the Configuration MODE resistors have to be re-soldered before to M2=1, M1=0, M0=1.
2) To configure the FPGA chips directly by VME the Configuration MODE resistors have to be re-soldered before to M2=1, M1=1, M0=1. This method also cannot configure the ROP and VME64 chip.

Configuration Mode	M2	M1	M0	CCLK Direction	Data Width	Dout
MasterSerial	**0**	**0**	**0**	**out**	**1**	**yes**
Slave Serial	1	1	1	in	1	yes
Master SelectMAP	0	1	1	out	8	no
Slave SelectMAP	1	1	0	in	8	no
Boundary Scan	**1**	**0**	**1**	**N/A**	**1**	**no**

Table 1 Configuration Modes for Virtex2 FPGAs

3.1.1 Default Configuration of FPGAs from PROMs

The FPGAs are set to **MASTER SERIAL** mode.

3.1.1.1 VME64 chip

- POWER UP At power-up the Chip is configured automatically from PROM

3.1.1.2 ROP chip

- POWER UP At power-up the Chip is configured automatically from PROM
- NSYSRES crate reset

3.1.1.3 INx, LFx, AUx, SRT chips

- POWER UP At power-up the Chip is configured automatically from PROM
- V_NPROG VME command start a reconfiguration
- NSYSRES crate reset

3.1.2 New permanent configuration file ➔ PROMs

New permanent configuration files are loaded into PROMs using JTAG.

3.1.2.1 VME64 Prom

- Byte Blaster ➔ JTAG CHAIN_A
- Backplane-JTAG (altera) ➔ JTAG CHAIN_A (=future option)

3.1.2.2 INx, LFx, AUx, SRT and ROP Proms

****** Exclude the FPGA chips from the JTAG chain!! ******

- Parallel Cable IV ➔ JTAG CHAIN_X
- VME-JTAG from ROP ➔ JTAG CHAIN_X
    - ROP-FPGA is skipped by jumpers (default position).
    - Other FPGAs might also be skipped by jumpers.
    - After reconfiguration from Proms (power-up, NSYSREs) the former design is lost.
    - ROP is used to change it's own logic circuits.
- Backplane-JTAG (xilinx) ➔ JTAG CHAIN_X (=future option)

3.1.3 Alternative FPGA configuration methods

Alternative FPGA configuration methods might be used during hardware tests. The configuration mode SMD-jumpers have to be soldered accordingly.

3.1.3.1 VME64

Set VME64 chip to JTAG mode.

- Byte Blaster ➔ JTAG CHAIN_A

3.1.3.2 ROP

Set ROP chip to JTAG mode.

- Parallel Cable IV ➔ JTAG CHAIN_X with ROP chip included.

3.1.3.3 INx, LFx, AUx, SRT

Set FPGAs to JTAG mode:

- Parallel Cable IV ➔ JTAG CHAIN_X
- VME-JTAG from ROP ➔ JTAG CHAIN_X with ROP chip skipped to avoid a crash.

Set FPGAs to SLAVE SERIAL mode:

- VME with CONFIG-Signals (CCLK, NPROG, DIN…) from ROP chip.
    - Set INx, LFx, Aux, SRT before to **SLAVE** mode by soldering on the MEZZ896 board the SMD-RESISTORS M2=M1=M0=HIGH.

3.1.4 JTAG Chains on GMT board

CHAIN_A: VME64x and its Proms <== ByteBlaster or Backplane-JTAG
CHAIN_X: INx, LFx, , AUx, SRT, ROP and their PROMS are controlled by
<== VME_JTAG, ParallelCableIV or Backplane-JTAG

The ROP chip will be skipped to keep it running during VME_JTAG configuration.

3.2 RESET concept

The following points show all reset options for the GMT in the Global Trigger crate.

3.2.1 POWER OFF and ON

To switch the GT-crate off is the last option to reset non-working Global Trigger electronics.

3.2.2 NSYSRES ➔ configuration of FPGAs

The common crate reset signal NSYSRES starts the configuration procedure for all FPGAs except the VME64 chip. It pulls the NPROG net to a low voltage level forcing each FPGA (master) to reconfigure from Proms.

3.2.3 RESET_DCM_xxx

ROP sends 9 signals **RESET_DCM_xxx** to the FPGAs (INx, LFx, Aux, SRT) resetting the DCM units and therefore re-synchronising the chips to the board CLK.

The DCM unit of ROP cannot be reset. In case of problems the ROP chip has to be reconfigured by NSYSRES = crate reset.

Net name	From ROP pins	To xxx pins
RESET_DCM_AUF	F16	AUF: AJ19
RESET_DCM_LFF	C16	LFF: AK17
RESET_DCM_LFB	**D17 ok**	LFB: AH18
RESET_DCM_AUB	**J16 ok**	AUB: AJ19
RESET_DCM_SRT	F17	SRT: AH19
RESET_DCM_INB	**J17 ok**	INB: AG17
RESET_DCM_IND	**G17 ok**	IND: AG17
RESET_DCM_INC	**H17 ok**	INC: AG17
RESET_DCM_INF	C15	INF: AG17

3.2.4 RESET_xxx and INACTIVE ➔STARTUP

The ROP chip sends 9 RESET_xxx signals to the FPGAs (INx, LFx, AUx, SRT) to reset the STARTUP modules inside the chips and the common INACTIVE signal enables the IO-pins to switch from high-Z to active mode.

RESET_xx ➔ GSR pin of STARTUP
INACTIVE ➔ GTS pin of STARTUP

The RESET_xx should reload the initial default values into all registers.

3.2.5 L1RES, BCRES, L1A ➔ reset State Machines and Counters

The Trigger Control System sends via the backplane the signals L1RES, BCRES, L1A and Event Counter Reset to reset state machines and counters.

3.2.6 VME commands ➔ reset State Machines and Counters

Also VME commands can be used to reset logic circuits inside the FPGAs.

3.3 Configuration at Power-UP and by SYSREST*

Power-Up respectively NPROG=low keep clearing configuration memory of the chip. After 2 memoring clearing cycles. The chip waits until NINIT has been released and becomes high. Then the Master serial CCLK begins loading the configuration data into the FPGA. If the CRC check finds an error afterwards the NINIT will be pulled low and startup aborted. If CRC check is ok the STARTUP sequence switches the chip into the operational mode.

3.4 Status monitoring

The INx, LFx, AUx, SRT chips send their **DCM_LOCKED** status signals and **2 STATUS bits** to the ROP chip. The ROP chip combines all status signals to a common 4 bit status code and sends the error code if a FPGA has lost synchronisation to the 40 MHz clock.
The 4 bit STATUS bits go via the backplane to the FDL board. On the FDL board the states of all boards are combined and the result is sent as the GT-crate status to the central trigger control board TCS.
The ROP writes the DCM locked signals and the STATUS bits into a status register that can be accessed by VME software.
A front panel LED shows also the combined status of the DCM_LOCKED signals.

3.4.1 Combining status signals

Each GMT chip sends 2 coded status bits to the ROP chip according to the table below.

Code	Status with examples
00	All ok
01	Warning buffer overflow (75% full derandomizing buffer)
10	Out_of sync: BC-cntr error, Derand-Buffer not empty at same time….etc
11	Error or FPGA is not configured (Pull-up resistors provide ‘11’.)

First the 2 bit codes are decoded back to singles state bits. The warning, out_of_sync and error states of all chips are ‘OR’ed. The inverted DCM_LOCKED_xx signals are also included as a error bits. The ROP chip provides the BUSY and READY state as set by the software. Then the results are coded again into a 4-bit code to be sent to the FDL board.

The following states can be formed with the following 4-bit code:

0001 WARNING // = OR of all warnings from INx, SRT and ROP chip
0010 OUT_OF_SYNC // =OR of all GMT chips
0100 BUSY // = set by VME software (CMD_REG in ROP chip)
1000 READY // = set by VME software (CMD_REG in ROP chip)
1100 ERROR // = OR of all GMT chips

A priority logic sends only the status with highest rank as a 4 bit code to the FDL board.
Highest priority: ERROR
2nd rank: OUT_OF_SYNC
3rd rank: BUSY
4th rank: WARNING
Lowest rank: READY

The Global Muon Trigger does not use other codes, which would be interpreted on the FDL board as ‘BAD CODE’. If the ROP chip is not configured or if the GMT board is not inserted then the FDL board receives either ‘0000’ or ‘1111’ as the ‘DISCONNECTED’ status.

4 VME_ROP chip

5 IN chips

6 LOGIC chips

7 Assignment Unit chips

8 Sorter chip

9 Test Procedures

10 MIP/ISO bits from GCT➔PSB➔GMT

		-6	-5	-4	-3	-2	-1	0
	0	3_6_0	3_45_1	3_45_0	1_23_1	1_23_0	1_01_1	1_01_0
	1	3_6_1	3_45_3	3_45_2	1_23_3	1_23_2	1_01_3	1_01_2
	2	3_6_8	3_45_9	3_45_8	1_23_9	1_23_8	1_01_9	1_01_8
	3	3_6_9	3_45_11	3_45_10	1_23_11	1_23_10	1_01_11	1_01_10
	4	4_6_4	4_45_5	4_45_4	2_23_5	2_23_4	2_01_5	2_01_4
	5	4_6_5	4_45_7	4_45_6	2_23_7	2_23_6	2_01_7	2_01_6
	6	7_6_0	7_45_1	7_45_0	5_23_1	5_23_0	5_01_1	5_01_0
	7	7_6_1	7_45_3	7_45_2	5_23_3	5_23_2	5_01_3	5_01_2
	8	7_6_8	7_45_9	7_45_8	5_23_9	5_23_8	5_01_9	5_01_8
	9	7_6_9	7_45_11	7_45_10	5_23_11	5_23_10	5_01_11	5_01_10
	10	8_6_4	8_45_5	8_45_4	6_23_5	6_23_4	6_01_5	6_01_4
	11	8_6_5	8_45_7	8_45_6	6_23_7	6_23_6	6_01_7	6_01_6
	12	11_6_0	11_45_1	11_45_0	9_23_1	9_23_0	9_01_1	9_01_0
	13	11_6_1	11_45_3	11_45_2	9_23_3	9_23_2	9_01_3	9_01_2
	14	11_6_8	11_45_9	11_45_8	9_23_9	9_23_8	9_01_9	9_01_8
	15	11_6_9	11_45_11	11_45_10	9_23_11	9_23_10	9_01_11	9_01_10
	16	12_6_4	12_45_5	12_45_4	10_23_5	10_23_4	10_01_5	10_01_4
phi	17	12_6_5	12_45_7	12_45_6	10_23_7	10_23_6	10_01_7	10_01_6

0	1	2	3	4	5	6
1_01_4	1_01_5	1_23_4	1_23_5	3_45_4	3_45_5	3_6_4
1_01_6	1_01_7	1_23_6	1_23_7	3_45_6	3_45_7	3_6_5
2_01_0	2_01_1	2_23_0	2_23_1	4_45_0	4_45_1	4_6_0
2_01_2	2_01_3	2_23_2	2_23_3	4_45_2	4_45_3	4_6_1
2_01_8	2_01_9	2_23_8	2_23_9	4_45_8	4_45_9	4_6_8
2_01_10	2_01_11	2_23_10	2_23_11	4_45_10	4_45_11	4_6_9
5_01_4	5_01_5	5_23_4	5_23_5	7_45_4	7_45_5	7_6_4
5_01_6	5_01_7	5_23_6	5_23_7	7_45_6	7_45_7	7_6_5
6_01_0	6_01_1	6_23_0	6_23_1	8_45_0	8_45_1	8_6_0
6_01_2	6_01_3	6_23_2	6_23_3	8_45_2	8_45_3	8_6_1
6_01_8	6_01_9	6_23_8	6_23_9	8_45_8	8_45_9	8_6_8
6_01_10	6_01_11	6_23_10	6_23_11	8_45_10	8_45_11	8_6_9
9_01_4	9_01_5	9_23_4	9_23_5	11_45_4	11_45_5	11_6_4
9_01_6	9_01_7	9_23_6	9_23_7	11_45_6	11_45_7	11_6_5
10_01_0	10_01_1	10_23_0	10_23_1	12_45_0	12_45_1	12_6_0
10_01_2	10_01_3	10_23_2	10_23_3	12_45_2	12_45_3	12_6_1
10_01_8	10_01_9	10_23_8	10_23_9	12_45_8	12_45_9	12_6_8
10_01_10	10_01_11	10_23_10	10_23_11	12_45_10	12_45_11	12_6_9

Tables show the MIP/ISO bit assignment into cables for both sides of CMS.
Horizontal: ETA values between -6….+6
Vertical: PHI values 0….17 (20° units)
Syntax: **CableNr_EtaValues_BitNumberOnCable(starting with zero)**

PSB board ➔ BACKPLANE ➔ GMT

CH7_6: bit 31: CON1_19e – bit0: CON2_12d bit31-16 ➔ MEM7, bit15-0 ➔ MEM6
CH5_4: bit 31: CON2_15e – bit0: CON3_5d bit31-16 ➔ MEM5, bit15-0 ➔ MEM4
CH3_2: bit 31: CON4_1e – bit0: CON4_16d bit31-16 ➔ MEM3, bit15-0 ➔ MEM2
CH1_0: bit 31: CON5_1e – bit0: CON5_16d bit31-16 ➔ MEM1, bit15-0 ➔ MEM0

PSB in SLOT19:

blue number = bit# in PSB. The empty PSB bits are not connected to the GMT board.

MEM7 ➔ bit31-16, MEM6 ➔ bit15-0

30	31
MQB4_45_8	MQB4_45_10
MQB4_45_4	MQB4_45_6
MQB4_45_0	MQB4_45_2
22	23
MQF4_6_8	MQF4_6_9
MQF4_6_4	MQF4_6_5
MQF4_6_0	MQF4_6_1
14	15
12	13
MQF4_45_10	MQF4_45_11
MQF4_45_8	MQF4_45_9
MQF4_45_6	MQF4_45_7
MQF4_45_4	MQF4_45_5
MQF4_45_2	MQF4_45_3
MQF4_45_0	MQF4_45_1

MEM3 ➔ bit31-16, MEM2 ➔ bit15-0

30	31
28	29
MQB2_23_10	MQB2_23_11
MQB2_23_8	MQB2_23_9
MQB2_23_6	MQB2_23_7
MQB2_23_4	MQB2_23_5
MQB2_23_2	MQB2_23_3
MQB2_23_0	MQB2_23_1
14	15
12	13
MQB2_01_10	MQB2_01_11
MQB2_01_8	MQB2_01_9
MQB2_01_6	MQB2_01_7
MQB2_01_4	MQB2_01_5
MQB2_01_2	MQB2_01_3
MQB2_01_0	MQB2_01_1

MEM5 ➔ bit31-16, MEM4 ➔ bit15-0

30	31
MQB3_45_8	MQB3_45_10
MQB3_45_4	MQB3_45_6
MQB3_45_0	MQB3_45_2
22	23
MQF3_6_8	MQF3_6_9
MQF3_6_4	MQF3_6_5
MQF3_6_0	MQF3_6_1
14	15
12	13
MQF3_45_10	MQF3_45_11
MQF3_45_8	MQF3_45_9
MQF3_45_6	MQF3_45_7
MQF3_45_4	MQF3_45_5
MQF3_45_2	MQF3_45_3
MQF3_45_0	MQF3_45_1

MEM1 ➔ bit31-16, MEM0 ➔ bit15-0

30	31
28	29
MQB1_23_10	MQB1_23_11
MQB1_23_8	MQB1_23_9
MQB1_23_6	MQB1_23_7
MQB1_23_4	MQB1_23_5
MQB1_23_2	MQB1_23_3
MQB1_23_0	MQB1_23_1
14	15
12	13
MQB1_01_10	MQB1_01_11
MQB1_01_8	MQB1_01_9
MQB1_01_6	MQB1_01_7
MQB1_01_4	MQB1_01_5
MQB1_01_2	MQB1_01_3
MQB1_01_0	MQB1_01_1

PSB in SLOT20:

MEM7 ➔ bit31-16, MEM6 ➔ bit15-0

30	31
MQB8_45_8	MQB8_45_10
MQB8_45_4	MQB8_45_6
MQB8_45_0	MQB8_45_2
22	23
MQF8_6_8	MQF8_6_9
MQF8_6_4	MQF8_6_5
MQF8_6_0	MQF8_6_1
14	15
12	13
MQF8_45_10	MQF8_45_11
MQF8_45_8	MQF8_45_9
MQF8_45_6	MQF8_45_7
MQF8_45_4	MQF8_45_5
MQF8_45_2	MQF8_45_3
MQF8_45_0	MQF8_45_1

MEM3 ➔ bit31-16, MEM2 ➔ bit15-0

30	31
28	29
MQB6_23_10	MQB6_23_11
MQB6_23_8	MQB6_23_9
MQB6_23_6	MQB6_23_7
MQB6_23_4	MQB6_23_5
MQB6_23_2	MQB6_23_3
MQB6_23_0	MQB6_23_1
14	15
12	13
MQB6_01_10	MQB6_01_11
MQB6_01_8	MQB6_01_9
MQB6_01_6	MQB6_01_7
MQB6_01_4	MQB6_01_5
MQB6_01_2	MQB6_01_3
MQB6_01_0	MQB6_01_1

MEM5 ➔ bit31-16, MEM4 ➔ bit15-0

30	31
MQB7_45_8	MQB7_45_10
MQB7_45_4	MQB7_45_6
MQB7_45_0	MQB7_45_2
22	23
MQF7_6_8	MQF7_6_9
MQF7_6_4	MQF7_6_5
MQF7_6_0	MQF7_6_1
14	15
12	13
MQF7_45_10	MQF7_45_11
MQF7_45_8	MQF7_45_9
MQF7_45_6	MQF7_45_7
MQF7_45_4	MQF7_45_5
MQF7_45_2	MQF7_45_3
MQF7_45_0	MQF7_45_1

MEM1 ➔ bit31-16, MEM0 ➔ bit15-0

30	31
28	29
MQB5_23_10	MQB5_23_11
MQB5_23_8	MQB5_23_9
MQB5_23_6	MQB5_23_7
MQB5_23_4	MQB5_23_5
MQB5_23_2	MQB5_23_3
MQB5_23_0	MQB5_23_1
14	15
12	13
MQB5_01_10	MQB5_01_11
MQB5_01_8	MQB5_01_9
MQB5_01_6	MQB5_01_7
MQB5_01_4	MQB5_01_5
MQB5_01_2	MQB5_01_3
MQB5_01_0	MQB5_01_1

The empty PSB bits are not connected to the GMT board.

PSB in SLOT21:

MEM7 ➔ bit31-16, MEM6 ➔ bit15-0

30	31
MQB12_45_8	MQB12_45_10
MQB12_45_4	MQB12_45_6
MQB12_45_0	MQB12_45_2
22	23
MQF12_6_8	MQF12_6_9
MQF12_6_4	MQF12_6_5
MQF12_6_0	MQF12_6_1
14	15
12	13
MQF12_45_10	MQF12_45_11
MQF12_45_8	MQF12_45_9
MQF12_45_6	MQF12_45_7
MQF12_45_4	MQF12_45_5
MQF12_45_2	MQF12_45_3
MQF12_45_0	MQF12_45_1

MEM3 ➔ bit31-16, MEM2 ➔ bit15-0

30	31
28	29
MQB10_23_10	MQB10_23_11
MQB10_23_8	MQB10_23_9
MQB10_23_6	MQB10_23_7
MQB10_23_4	MQB10_23_5
MQB10_23_2	MQB10_23_3
MQB10_23_0	MQB10_23_1
14	15
12	13
MQB10_01_10	MQB10_01_11
MQB10_01_8	MQB10_01_9
MQB10_01_6	MQB10_01_7
MQB10_01_4	MQB10_01_5
MQB10_01_2	MQB10_01_3
MQB10_01_0	MQB10_01_1

MEM5 ➔ bit31-16, MEM4 ➔ bit15-0

30	31
MQB11_45_8	MQB11_45_10
MQB11_45_4	MQB11_45_6
MQB11_45_0	MQB11_45_2
22	23
MQF11_6_8	MQF11_6_9
MQF11_6_4	MQF11_6_5
MQF11_6_0	MQF11_6_1
14	15
12	13
MQF11_45_10	MQF11_45_11
MQF11_45_8	MQF11_45_9
MQF11_45_6	MQF11_45_7
MQF11_45_4	MQF11_45_5
MQF11_45_2	MQF11_45_3
MQF11_45_0	MQF11_45_1

MEM1 ➔ bit31-16, MEM0 ➔ bit15-0

30	31
28	29
MQB9_23_10	MQB9_23_11
MQB9_23_8	MQB9_23_9
MQB9_23_6	MQB9_23_7
MQB9_23_4	MQB9_23_5
MQB9_23_2	MQB9_23_3
MQB9_23_0	MQB9_23_1
14	15
12	13
MQB9_01_10	MQB9_01_11
MQB9_01_8	MQB9_01_9
MQB9_01_6	MQB9_01_7
MQB9_01_4	MQB9_01_5
MQB9_01_2	MQB9_01_3
MQB9_01_0	MQB9_01_1

The empty PSB bits are not connected to the GMT board.